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ABSTRACT

This guide contains instructor's materials for a 10-unit secondary school course on digital logic application. The units are introduction to digital, logic gates, digital integrated circuits, combination logic, flip-flops, counters and shift registers, encoders and decoders, arithmetic circuits, memory, and analog/digital and digital/analog conversions. The document begins with advice on its use and a cross-referenced table of instructional materials that show which materials in the guide (transparency masters, handouts, assignment sheets, and test items) are directed at which competencies and instructional objectives. Each unit contains the unit objective, student objectives, a list of references, notes to the instructor, lesson plans, a unit test, and answers to the unit test. The lesson plans may include a glossary, information sheets, transparency masters, job sheets, assignment sheets, and test items. (CML)

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Instructor's Guide

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ELECTRONICS
Module

3

DIGITAL LOGIC APPLICATION

CE 054 378

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ELECTRONICS

Module 3: Digital Logic Application

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1989

Instructor's Guide
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FOREWORD

Once again, we are indebted to the teachers and administrators who provide their time, efforts and professionalism to develop curriculum for trade, technical and industrial education programs. This electronics guide is an outstanding example of what can be accomplished when the right people with the right attitude get together. Committee members worked hard over several years' time in advisory, writing, technical consultation and field-test capacities.

This guide is designed to be totally integrated with the Vocational Instructional Management System. It is hoped that all guides produced under our supervision will help classroom teachers manage instruction. A curriculum guide is more than a resource--it is an integral part of the management system. Rather than impeding instruction, it should guide and facilitate instruction.

This guide's format has been set up for competency-based teaching and testing. Unit tests evaluate specific competencies and can be used with the Vocational Administrative Management System (VAMS). Information sheets, transparency masters, job sheets, assignment sheets and test items are keyed to specific competencies. A cross-reference table has been included to quickly identify parts of the curriculum that relate to specific competencies. The material has also been packaged for students.

Although this guide may be a new format for some teachers, we are confident that, when used as designed, time spent by teachers and students will become more productive. Any future electronics curriculum modifications will begin with this guide. The electronics field is undergoing constant and considerable change. We will annually evaluate the need to update this guide on a module-by-module basis. Your suggestions regarding areas for improvement are both encouraged and appreciated.

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ACKNOWLEDGMENTS

This electronics guide represents a continuing commitment to Missouri's Vocational Instructional Management System (VIMS). The guide has been keyed to the electronics competency profile developed by industry and education professionals in the state.

When searching for current electronics materials to adopt or utilize in the guide's development, comparable materials were found from the Mid-America Vocational Curriculum Consortium (MAVCC), of which Missouri is a member. MAVCC materials, therefore, have been relied upon as a resource for this guide. A debt of thanks is owed to the entire MAVCC organization for the research and development of these electronics materials.

Special appreciation is given to the writers (Ed Carter, John Chappell, Jim Everett, Bill Franken, Mark Murphy, Don Slack and Bill Tharp) for their self-motivation, reliability and technical expertise. IML employees Crystal Dietiker and Donna Curtis contributed greatly to the guide's production.

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Crystal Dietiker, graphic artist II
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COMPETENCIES ADDRESSED IN THIS MODULE

K. Digital Logic Application

1. Identify and convert number systems and codes for binary, hex, octal and BCD
2. Identify and describe the operation of basic logic gates
3. Develop truth tables defining circuit design
4. Test and repair logic circuits
5. List advantages and disadvantages of SSI, MSI, LSI and VLSI
6. Describe the characteristics of ROM's and PLA's
7. Construct combination logic circuits for a given application
8. Describe digital counter operating modes and their function
9. Construct counter and controller circuits for sequential logic applications
10. Describe the advantages of test instruments that use digital techniques
11. Use data sheets
12. Describe the operation of A/D and D/A convertors

H. Test Equipment

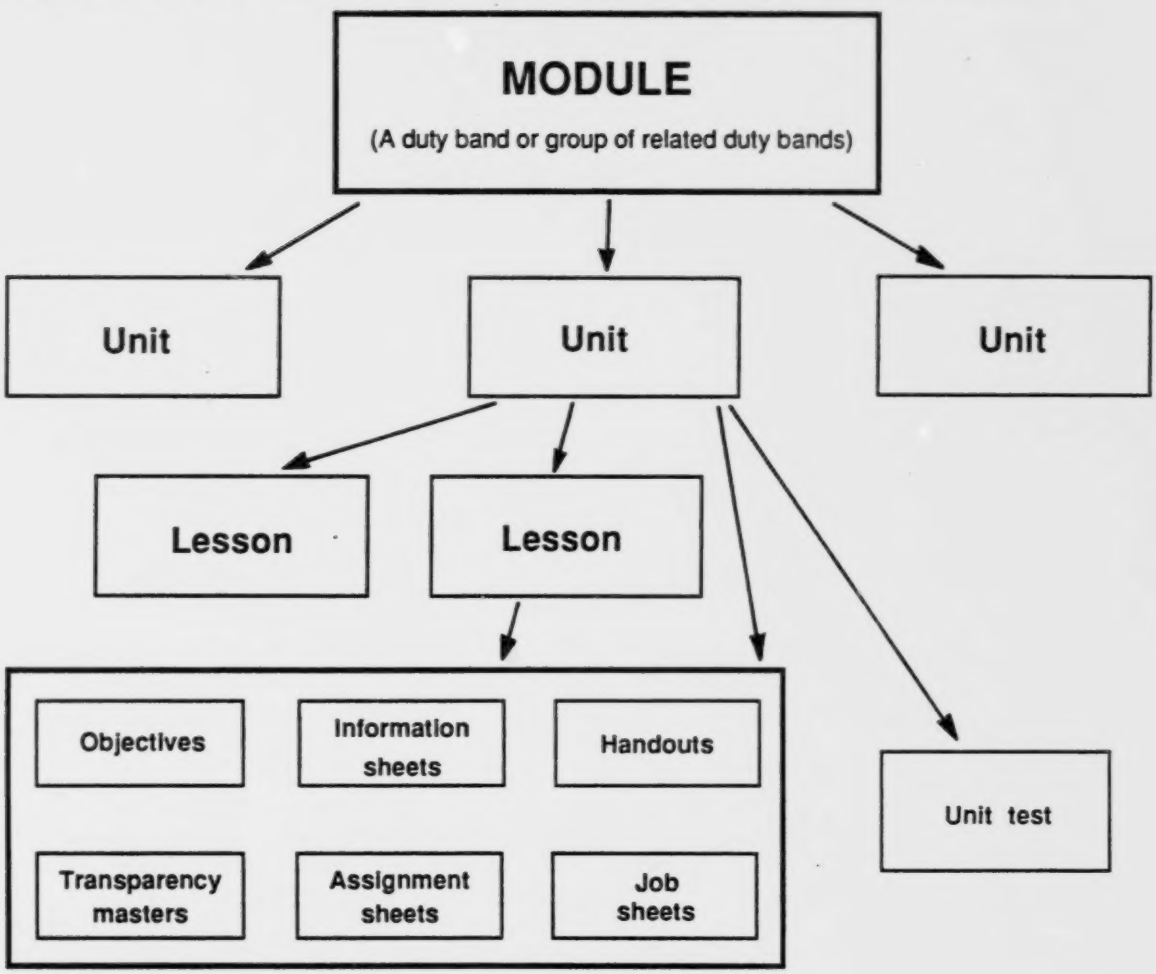
6. Describe the operation and demonstrate the use of logic probes

HOW TO USE THIS PUBLICATION

GUIDE COMPONENTS

Units of instruction

This Electronics guide contains ten modules of instruction. Within each module are instructional units including some or all of the following components: performance objectives, information sheets, transparency masters, handouts, assignment sheets, job sheets and a unit test. Special instructions on audiovisuals, supplies, etc. are included in the Notes to the Instructor section near the beginning of each unit.



Competency profile

On the Missouri competency profile, tasks are divided into general subject areas, or duty bands, which are identified by a capital letter. Under each duty band are related tasks (competencies), which are identified by an Arabic numeral. To evaluate the student on performance of the competencies, a 3-2-1-N grading system is used, where:

- **3 = Mastery** - can work independently with no supervision
- **2 = Requires supervision** - can perform job completely with limited supervision
- **1 = Not mastered** - requires instruction and close supervision
- **N = No exposure** - no experience or knowledge in this area

Cross-reference table (color-coded white)

Once the numbering system is understood, this table quickly reveals how the instructional components of the module relate to Missouri competencies. On the competency profile, tasks are divided into general subject areas, or duty bands, which are identified by a capital letter. Under each duty band are related tasks (competencies), which are identified by an Arabic numeral.

On the cross-reference table, unit numbers are represented by Roman numerals (I, II, III, etc.). Lessons within a unit are shown with Arabic numerals. Therefore, the first objective in Lesson 1 is numbered 1.1, the second is 1.2, and so on. Other components of the module (transparencies, handouts, assignment sheets and job sheets) also use this numbering system. By looking at the cross-reference table, the instructor can quickly determine what test questions or job sheets a student needs to receive an evaluation on a particular competency.

Objectives (color-coded white)

Each unit is based on performance objectives which state the measurable unit and specific behavioral or performance objectives that students are expected to achieve. Since the objectives of the unit provide direction for the teaching-learning process, it is important for the teacher and students to have a common understanding of the objectives' intent. Teachers should feel free to add/adapt objectives which will fit the material to student and community needs. Supporting material will, of course, need to be added for any new objectives.

Table of contents, references, notes to the instructor (color-coded pink)

These pages have been coded pink for instructor use only. The reference section lists materials used as sources in developing the material. Special instructions on audiovisuals, supplies, etc. are included in the Notes to the Instructor section.

Information sheets (green)

Presented in outline form for clarity, these pages provide content essential for meeting the cognitive (knowledge) objectives in the unit. Students should study the information sheets before class discussion or completion of assignment sheets. **CAUTION** statements indicate possible equipment damage, while **WARNING** statements recommend procedures to avoid bodily injury. Handouts and transparency masters have been keyed in the information sheets for instructional use.

Transparency masters (white)

Transparencies provide information by visually reinforcing or clarifying ideas presented in the information sheets. They are effective when identification is necessary and direct the class's attention to the topic of discussion. Transparencies should be left on the screen only when topics shown are under discussion, however.

Handouts (white)

Whenever more detailed information than can be presented in a transparency is needed, a handout is used. Handouts give the students additional information that can be kept with their class notes or student references.

Assignment sheets (tan)

Assignment sheets furnish paper-and-pencil practice to develop the knowledge necessary as a prerequisite to skill development. They can be given to students for class completion or used as homework assignments. Answer sheets (color-coded pink) can be used by the student or instructor to check progress.

Job sheets (blue)

These evaluation instruments are provided for two purposes: to outline steps of procedure and to check student performance mastery. Job sheets begin with a list of tools and materials needed for the activity. Job sheets furnish potential employers with a picture of skills being taught and performance which might

be reasonably expected from a vocational student. The spaces to the right of the page on a job sheet assist the instructor in evaluating a student on a particular activity. This 3-2-1-N grading system is the same as the one used on the competency profile.

Unit test (yellow)

Competency-based tests are designed to help eliminate subjective testing and to improve student evaluation and accountability. Specific competencies and test questions are linked on the answer key. These welding unit tests have been written to be used with computerized VAMS (Vocational Administrative Management System), utilizing Scantron sheets for computer-recording of test answers.

The unit test may be eliminated if the competency was thoroughly evaluated by job sheets. However, an emphasis should be placed on cognitive as well as performance skills. If the objective or competency will be evaluated by a job sheet, it is often necessary to determine by a written test whether the student understands enough of the material to perform the job sheet.

SUGGESTED ACTIVITIES

The following list of suggested activities may be helpful, especially to the beginning instructor.

1. Provide students with objective sheet and information sheets.
2. Discuss unit and specific objectives.
3. Discuss information sheets, assignment sheets and/or job sheets, lesson-by-lesson.
4. Have students do assignment sheet(s) to satisfactory levels.
5. Give students unit test.
6. After successful completion of the test, have students do job sheet(s).

Students should perform the following activities.

1. Read objective sheet.
2. Study information sheets.
3. Do assignment sheet(s).
4. Take unit test.
5. Do job sheets.

PACKAGING

This Electronics guide has been packaged with the entire class in mind. For the teacher, a complete instructor's guide contains all ten modules. In the student reference, selected portions have been reproduced for student use (objectives page, information sheets, handouts). Student work sheets (assignment sheets, job sheets, unit tests) have been packaged together for student distribution as the instructor deems necessary.

In the student reference, page numbers do not run consecutively because some pages have been removed that appear only in the instructor's guide.

MODULE 3: DIGITAL LOGIC APPLICATION

CROSS-REFERENCE TABLE OF INSTRUCTIONAL MATERIALS

Competency	Instructional Objective	Transparency Master	Handout	Assignment Sheet	Job Sheet	Test Item	Notes
K1	I 1.3-1.5		I 1.2	I 1.2		I 1,5-8,10-20	
K2	II 1.3,1.4,1.6		II 1.1	II 1.1	II 1.1	II 2-8,10,12-22	
K3	II 1.3		II 1.1	II 1.1, V 1.1	IV 2.1, V 1.4		
K4	VII 1.1,1.2,2.1-2.3, X 1.4,2.4			VII 1.1,2.1,2.2	VII 1.1,2.1, X 1.4,2.4	VII 1-10	
K5	III 1.1-1.3, 2.1,2.2			III 1.1, 2.1		III 1-20	
K6	IX 1.1-1.5,2.1-2.4				IX 1.1	IX 1-24	See Notes to the Instructor
K7	IV 1.1,1.2,2.1,2.2, V 1.1-1.5, VIII 1.1-1.4,2.1-2.4, 3.1-3.3			IV 1.1,2.1, V 1.1	IV 2.1, V 1.1-1.4, VIII 1.1, 2.1,3.1	IV 1-10, V 1-12, VIII 1-7,11-14	
K8	VI 1.1,1.2,1.4,1.5, 1.7,2.1-2.4			VI 1.1		VI 1-18	
K9	VI 1.3, 1.6		VI 2.1	VI 2.1	VI 1.1, 1.2,2.1		
K10	I 1.1-1.2		I 1.1	I 1.1		I 1-4,9	
K11	IX 1.5, X 1.3		V 1.1, VI 1.1,2.1, X 1.1	III 1.2, VI 2.1, X 1.1	IX 1.1	VIII 8-10	
K12	X 1.1-1.4,2.2-2.4				X 1.1,1.2	X 1-17	
H6	VII 1.1,1.2,2.1-2.3				VII 1.1,2.1, VIII 1.1		

MODULE: DIGITAL LOGIC APPLICATION

UNIT 1: INTRODUCTION TO DIGITAL

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to discuss the advantages of digital electronics over analog electronics, identify digital and analog signals, and convert between various number systems. This knowledge will be evidenced by achieving the specified score on the unit test.

SPECIFIC OBJECTIVES

After completion of the lessons in this unit, the student should be able to:

1.1 Define terms and definitions.

1.2 Contrast analog and digital characteristics and signals. (competency K10)

1.3 Convert between binary, decimal, octal and hexadecimal number systems.

1.4 Identify characteristics of various binary codes.

1.5 Discuss ways data is represented in terms of logic levels and transmission types. (competency K1)

MODULE: DIGITAL LOGIC APPLICATION

UNIT I: INTRODUCTION TO DIGITAL

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plan

1. Lesson 1: INTRODUCTION TO DIGITAL

   a. Information outline

   b. Handouts

      HO 1.1: Analog vs. digital
      HO 1.2: American Standard Code for Information Interchange (ASCII)

   c. Assignment sheets

      AS 1.1: Analog vs. digital
      AS 1.2: Number systems

   d. Answers to assignment sheets

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. Digital Techniques (Book 1 and 2). Benton Harbor, MI: Heath Co., 1986.

2. Forbes, Mark, and Barry B. Brey. Digital Electronics. Indianapolis, IN: Bobbs-Merrill Educational Publishing, 1984.

3. Graf, Rudolf F. Modern Dictionary of Electronics. 6th ed. Indianapolis, IN: Howard W. Sams & Co., Inc., 1984.

NOTES TO THE INSTRUCTOR

A. Suggested student activities

1. Have students create 20 conversion problems and answers. Then have them exchange problems, work the new problems and return completed answers to the students who created the problems. The students then grade the answers. The instructor resolves any answer disputes.

2. Students can translate a 5-10 word transmission into ASCII code including parity bit and indicating odd or even parity.

3. Draw the pulse train of the transmission in the above activity with five-volt and zero-volt logic levels, using both positive and inverted input logic.

B. Suggested supplemental audiovisual

1. Number Systems (E-89-360). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

MODULE: DIGITAL LOGIC APPLICATION

UNIT I: INTRODUCTION TO DIGITAL

LESSON 1: INTRODUCTION TO DIGITAL

I. Terms and definitions

A. Analog--pertaining to computers which create a physical (often electrical) likeness of the input; output represented smoothly and continuously

B. ASCII--(American Standard Code for Information Interchange) Pronounced "ask-ee," this standardized code uses 128 numerals, letters, symbols and special control codes represented by a seven-bit binary number.

C. BCD--(binary coded decimal) a special binary code used in some digital systems to make number systems easier to work with; system in which digits are in binary notation (0s and 1s)

D. Binary--based on two digits or numbers (0 and 1)

E. Binary number system--a Base 2 number system used in digital electronics

F. Decimal--based on 10 digits or numbers

G. Digital--pertaining to computers which store data by digits--usually binary; output is in discrete steps (pulses or on-off operations)

H. Logic level--voltage level assigned to a binary 1 and a binary 0

I. LSB--(least significant bit) right-most digit of a number; has the lowest value in the number

J. MSB--(most significant bit) left-most bit; has the highest order or greatest weight

II. Digital data

A. Useful electronic signals are mainly analog and digital. (HO 1.1)

1. Both are classified according to how the signal varies.

2. Analog signals vary smoothly and continuously. Examples: DC and AC voltage signals

3. Digital

a. Signals vary in discrete steps or increments. Most digital signals have two different levels, though some contain more levels.

b. Digital signals having two discrete levels are sometimes referred to as binary signals.

4. Conversion between signals

a. Analog-to-digital converter (ADC)--required to drive a digital circuit with an analog signal

b. Digital-to-analog converter (DAC)--required to drive an analog circuit with a digital signal

B. Analog vs. digital devices or quantities

1. Almost any device or quantity can be classified as analog or digital in nature.

2. Examples of analog quantities: time and temperature

   a. Both vary smoothly and continuously.

   b. Both are typically and traditionally measured with devices that are analog. (These are now also measured with digital devices.)

3. A slide rule is an analog device, whereas a calculator is a digital device because of the on-off nature of the displays and the discrete keys.

4. A light bulb is digital in nature if it is controlled by a switch, but it is analog if controlled by a potentiometer.

C. Advantages of digital electronics

1. Convenience: It is easy to read a current, voltage or resistance measurement from a digital display. (When measuring these same quantities on an analog meter, interpretation of the scale and possibly calculations must be made before the measurement is completed.)

2. Accuracy: Numbers are read directly. (Errors can be made while determining where the pointer is on an analog instrument.)

3. Low cost: Design costs are less, but implementation is subject to more cost due to conversion from "real world" analog to digital, i.e. temperature.

4. Simplicity of circuit design allows for new approaches to problems.

III. Number systems

A. Binary number system

1. Digital circuits process binary numbers.

2. The binary number system is a Base 2 number system--the 1 and 0 are the only binary digits (bits).

3. When converting a binary number to its decimal equivalent, add together the weights of the positions where a binary 1 occurs. (See example below.)

Positional notation:	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
Binary number:	1	0	0	1	0	1	1	1

2^7	=	128
2^4	=	16
2^2	=	4
2^1	=	2
2^0	=	+ 1
Decimal equivalent:		151

4. Conversion of a decimal number to its binary equivalent

   a. Repeatedly divide the number by two and note the remainder, which will always be a 1 or 0.

b. The first remainder is the LSB (least significant bit) (1's place) and the last remainder is the MSB (most significant bit).

c. Example:

150 ÷ 2 = 75	remainder	0	**LSB**
75 ÷ 2 = 37	remainder	1	
37 ÷ 2 = 18	remainder	1	
18 ÷ 2 = 9	remainder	0	
9 ÷ 2 = 4	remainder	1	
4 ÷ 2 = 2	remainder	0	
2 ÷ 2 = 1	remainder	0	
1--------> 1			**MSB**

5. Calculators are available which can convert among number systems, including the hexadecimal system (Base 16), which will be required later in the study of microprocessors.

6. To find the maximum number that can be represented with X number of bits, use the formula 2^X-1.

   Example: The maximum number that can be represented with eight bits is 255. (2^8 - 1 = 256 - 1 = 255)

7. To find the number of discrete or different states that can be represented with X number of bits, use the formula 2^X.

   NOTE: Do not subtract 1--0 is a number.

   Example: The number of discrete states that can be represented with 8 bits is 256. (There are from 0 to 255 discrete steps or increments, which is a total of 256 discrete states.)

B. Hexadecimal number system

1. The hexadecimal number system has a base or radix of 16. There are 16 discrete steps or states--0 through F.

   Hexadecimal: 0 1 2 3 4 5 6 7 8 9 A B C D E F_{16}

   Decimal: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15_{10}

2. To convert a hexadecimal number to its decimal equivalent, multiply the hexadecimal digit by the weighted position.

   Example: 16^1 16^0
   A F$_{16}$= _____ $_{10}$

   A (10) x 16^1 = 160
   \+ F (15) x 16^0 = 15
   175_{10}

3. Conversion of a decimal number to its hexadecimal equivalent

   a. Repeatedly divide by 16 and note the remainder.

   b. This is the same method used to convert decimal to binary, except that division is by 16 instead of 2.

c. Example: $175_{10} = AF_{16}$

175 ÷ 16 = 10 remainder 15 or hexadecimal F **LSB**
10 ----------> A **MSB**

4. To convert a hexadecimal number to its binary equivalent, treat each hexadecimal digit as four binary bits.

   Example: A = 1010 and F = 1111, therefore $AF_{16} = 10101111_2$

5. To convert a binary number to its hexadecimal equivalent, divide the binary number into four-bit numbers starting with the LSB. Then convert each four-bit number to the hexadecimal equivalent.

   Example: $11010011_2 = D3_{16}$ ($1101 = D$; $0011_2 = 3_{16}$)

C. Octal number system

1. The octal number system has a base or radix of eight (eight discrete steps or states).

2. When converting a decimal number to its octal equivalent, repeatedly divide by eight and note the remainder.

   Example: 132 ÷ 8 = 16 remainder 4 **LSB**
   16 ÷ 8 = 2 remainder 0
   2 --------> 2 **MSB**
   Therefore: $132_{10} = 204_8$

3. To convert an octal number to its decimal equivalent, multiply each octal digit by the positional notation.

   Example: $637_8 = 415_{10}$

   $6 \times 8^2 = 384$
   $3 \times 8^1 = 24$
   $+ \quad 7 \times 8^0 = 7$
   415

4. To convert an octal number to its binary equivalent, treat each octal digit as three binary bits.

   Example: $724_8 = 111010100_2$ (7 = 111, 2 = 010, 4 = 100)

5. When converting a binary number to its octal equivalent, divide the number into three-bit numbers starting with the LSB. Then convert each three-bit number to the octal equivalent.

   Example: $111010011_2 = 111\ 010\ 011_2 = 7\ 2\ 3 = 723_8$

IV. Binary codes

A. Binary coded decimal (BCD)

1. BCD uses four binary bits to represent one decimal digit. Since it only requires four binary bits (1001) to represent a 9, all nine decimal digits (0-9) can be created.

Decimal number:	9	6	5
BCD:	1001	0110	0101

2. BCD numbers can be identified by the spaces between numbers. Pure binary numbers do not have spaces between them.

3. The advantage of BCD over pure binary is that it is easier to determine the decimal equivalent of the number.

4. The disadvantage of BCD over pure binary is the number of bits used to represent each number. The decimal number 621 requires 12 bits in BCD, while the same number requires 10 bits in pure binary. This difference becomes greater as the decimal value increases.

B. XS3--a code in which the actual decimal equivalent is three greater than the pure binary number. This number system is used to simplify arithmetic operations.

C. Gray code--a non-weighted binary code that cannot be determined by calculations.

1. The LSB starts with one 0 and then has alternating patterns of two 1s and two 0s. The second-most significant bit starts with two 0s and then has alternating patterns of four 1s and four 0s.

   NOTE: Only one bit changes from one number to the next. This reduces errors.

2. The disadvantage of the Gray code is that it is difficult to determine the decimal equivalent of the number.

3. Gray code/binary code comparison

Decimal	Gray	Pure binary
0	0000	0000
1	0001	0001
2	0011	0010
3	0010	0011
4	0110	0100
5	0111	0101
6	0101	0110
7	0100	0111
8	1100	1000
9	1101	1001
10	1111	1010
11	1110	1011
12	1010	1100
13	1011	1101
14	1001	1110
15	1000	1111

D. ASCII (American Standard Code for Information Interchange) is an alphanumeric code used when communicating with computers, teletypes, CRT terminals, etc. (HO 1.2)

1. A binary-based code in which bit patterns represent letters of the alphabet, numbers and control characters

2. ASCII is a seven-bit code.

3. Variations of ASCII--Binary Coded Decimal Interchange Code (BCDIC), IBM's Extended Binary Code Decimal Interchange Code (EBCDIC), Selectric (used in IBM spinning ball printers and typewriters)

V. Data representation

A. Logic levels

1. Binary 1s and 0s are usually represented electronically by two discrete voltage levels.

2. Types of logic that can be used

a. In positive logic, the most positive voltage represents the binary 1.

b. In inverted input logic, the most negative voltage represents the binary 1.

c. Logic levels assigned to voltages

Positive logic	Inverted input logic
Binary 0 = +.2V	Binary 0 = +3.4V
Binary 1 = +3.4V	Binary 1 = +.2V
Binary 0 = -6V	Binary 0 = 0V
Binary 1 = 0V	Binary 1 = -6V
Binary 0 = +1V	Binary 0 = +15V
Binary 1 = +15V	Binary 1 = +1V

3. Sometimes, a binary 1 is referred to as a logic high and a binary 0 is referred to as a logic low.

B. Parallel vs. serial data transmission

1. Digital data can be represented in either serial or parallel form.

2. Serial data transmission

a. Requires only one hardware line

b. Data transmitted and received one bit after the other

c. Slow but less costly than parallel

3. Parallel data transmission

a. Binary words, transmitted in the form of parallel bits, are received at the same time.

b. Faster but more costly than serial

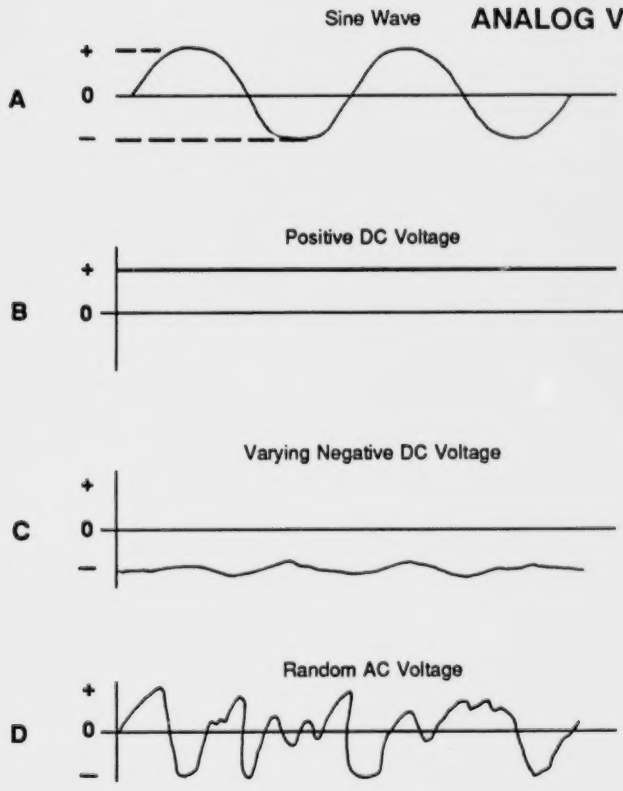
C. Devices used to represent logic levels

1. Any device that is digital in nature, such as a switch, can be used to implement the logic levels.

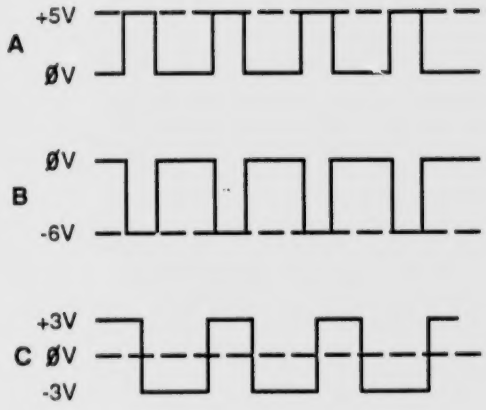
2. In saturation and cut-off regions of operation, the most common devices used to represent logic levels are bipolar and MOS (metal-oxide semiconductor) transistors.

3. Relays and magnetic cores can also be used to represent the two logic levels.

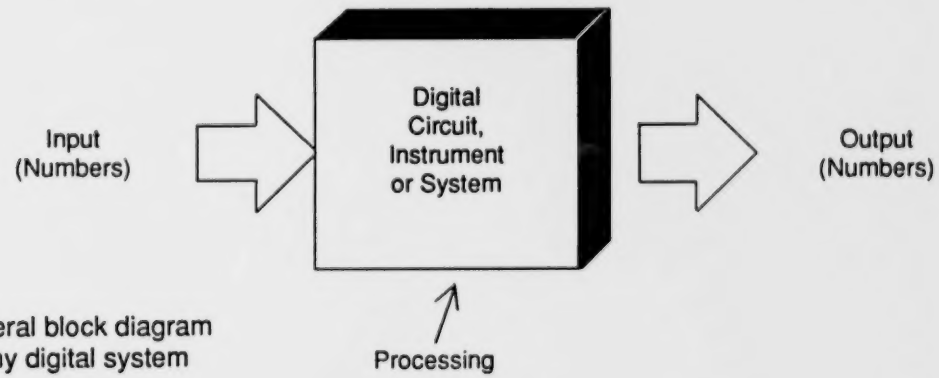
ANALOG VS. DIGITAL



Types of analog signals



Types of digital signals



A general block diagram of any digital system

Credit: Digital Techniques (Book 1). Benton Harbor, MI: Heath Co., 1986, pg. 1-6, 1-7 and 1-21.

AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)

ROW	COLUMN	0 (3)	1 (3)	2 (3)	3	4	5	6	7 (3)
	BITS 4321 765	000	001	010	011	100	101	110	111
0	0000	NUL	DLE	SP	0	@	P	\	p
1	0001	SOH	DC1	!	1	A	Q	a	q
2	0010	STX	DC2	"	2	B	R	b	r
3	0011	ETX	DC3	#	3	C	S	c	s
4	0100	EOT	DC4	$	4	D	T	d	t
5	0101	ENQ	NAK	%	5	E	U	e	u
6	0110	ACK	SYN	&	6	F	V	f	v
7	0111	BEL	ETB	'	7	G	W	g	w
8	1000	BS	CAN	(	8	H	X	h	x
9	1001	HT	EM	)	9	I	Y	i	y
10	1010	LF	SUB	*	:	J	Z	j	z
11	1011	VT	ESC	+	;	K	[	k	{
12	1100	FF	FS	,	<	L	\	l	¦
13	1101	CR	GS	–	=	M	]	m	}
14	1110	SO	RS	.	>	N	^ (1)	n	~
15	1111	SI	US	/	?	O	— (2)	o	DEL

Explanation of special control functions in columns 0, 1, 2 and 7.

NUL	Null
SOH	Start of Heading
STX	Start of Text
ETX	End of Text
EOT	End of Transmission
ENQ	Enquiry
ACK	Acknowledge
BEL	Bell (audible signal)
BS	Backspace
HT	Horizontal Tabulation (punched card skip)
LF	Line Feed
VT	Vertical Tabulation
FF	Form Feed
CR	Carriage Return
SO	Shift Out
SI	Shift In
SP	Space (blank)
DLE	Data Link Escape
DC1	Device Control 1
DC2	Device Control 2
DC3	Device Control 3
DC4	Device Control 4
NAK	Negative Acknowledge
SYN	Synchronous Idle
ETB	End of Transmission Block
CAN	Cancel
EM	End of Medium
SUB	Substitute
ESC	Escape
FS	File Separator
GS	Group Separator
RS	Record Separator
US	Unit Separator
DEL	Delete

Credit: Digital Techniques (Book 1). Benton Harbor, MI: Heath Co., 1986, pg. 1-35, 1-48.

ANALOG VS. DIGITAL

Define the following terms.

1. Analog:

2. Digital:

3. Draw two examples of analog signals and two examples of digital signals. Label each.

List three advantages of digital techniques over analog techniques.

4.

5.

6.

List three analog and three digital devices.

Analog	Digital

7.

8.

9.

Short answer

10. Binary is a base _____ number system, which means that the binary number system has _____ discrete states or increments.

11. Decimal is a base _____ number system, which means that the decimal number system has _____ discrete states or increments.

12. Which binary code is easy to translate into decimal numbers?

13. Which code is an alphanumeric code used in telecommunications?

14. Write the ASCII code for the name of your school.

15. Draw a square wave for the binary values in question #14 using positive logic.

16. Draw a square wave for the binary values in question #14 using inverted input logic.

17. Which type of data transmission (serial or parallel) is faster?

18. Which type of data transmission (serial or parallel) requires less hardware?

Identify the following acronyms in words.

19. BCD:

20. ASCII:

21. LSB:

22. MSB:

23. DAC:

24. ADC:

25. BCDIC:

26. EBCDIC:

NUMBER SYSTEMS

Convert the following numbers to the indicated number system. The subscripted values identify the base or radix of the number.

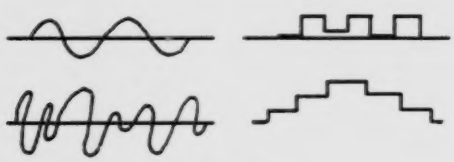
1. 141_{10} = _____ $_{2}$
2. 176_{8} = _____ $_{16}$
3. 255_{10} = _____ $_{2}$
4. 100_{16} = _____ $_{10}$
5. 222_{10} = _____ $_{2}$
6. AA_{16} = _____ $_{2}$
7. 121_{8} = _____ $_{10}$
8. 111_{10} = _____ $_{16}$
9. $F54_{16}$ = _____ $_{2}$
10. 255_{10} = _____ $_{16}$
11. 100_{8} = _____ $_{16}$
12. 222_{8} = _____ $_{2}$
13. FB_{16} = _____ $_{8}$
14. 1011101_{2} = _____ $_{16}$
15. 1000101_{2} = _____ $_{8}$
16. 1000100_{2} = _____ $_{10}$
17. 0011111_{2} = _____ $_{16}$
18. 1111111_{2} = _____ $_{10}$
19. 1010000_{2} = _____ $_{8}$
20. $1A_{16}$ = _____ $_{8}$

Short answer

21. Any binary number that has a one as the LSB is an (odd/even) number.
22. The maximum number that can be represented with eight binary digits (bits) is _____ .
23. There are _____ discrete states or steps in an eight-bit number.

ANSWERS TO AS 1.1

1. Varies smoothly and continuously
2. Varies in discrete or abrupt steps
3. Analog Digital



4-6. Three of the following:
Reliability
Accuracy
Range
New techniques
Cost

7-9. Analog:
Potentiometer
Weather vane
Slide rule

Digital:
Typewriter
Computer
Keyboard
Switch

10. 2, 2
11. 10, 10
12. BCD
13. ASCII
14-16. Evaluated by instructor
17. Parallel
18. Serial
19. Binary coded decimal
20. American Standard Code for Information Interchange
21. Least significant bit
22. Most significant bit
23. Digital-to-analog converter
24. Analog-to-digital converter
25. Binary Coded Decimal Interchange Code
26. Extended Binary Coded Decimal Interchange Code

ANSWERS TO AS 1.2

1.	10001101	9.	111101010100	17.	1F
2.	7E	10.	FF	18.	127
3.	11111111	11.	40	19.	120
4.	256	12.	10010010	20.	32
5.	1101110	13.	373	21.	Odd
6.	10101010	14.	5D	22.	255
7.	81	15.	105	23.	256
8.	6F	16.	68		

MODULE: DIGITAL LOGIC APPLICATION

UNIT I: INTRODUCTION TO DIGITAL

UNIT TEST

Choose the option which best answers the question or completes the statement.

___ 1. How many discrete steps or states are there in binary?

a. 1
b. 2
c. 8
d. 16
e. 18

___ 2. Which of the following is digital in nature?

a. Temperature
b. Potentiometer
c. Time
d. Switch
e. None of the above

___ 3. Which is <u>not</u> a characteristic of digital techniques?

a. Low cost
b. Convenience
c. High cost
d. Accuracy
e. All of the above

___ 4. Which is an acronym for a circuit that converts signals?

a. BCD
b. ADC
c. ASCII
d. BDC
e. All of the above

___ 5. Which number system has a base or radix of eight?

a. Binary
b. Octal
c. Decimal
d. Hexadecimal
e. Metric

___ 6. What is the BCD equivalent of the decimal number 679?

a. 0110 1001 1000
b. 0101 0111 1010
c. 0110 0111 1001
d. 0110 1000 1001
e. None of the above

___ 7. Which binary code is used for data communications?

a. ECBID
b. BCD
c. DAC
d. ADC
e. ASCII

___ 8. Which of the following codes is non-weighted?

a. Gray
b. BCD
c. DAC
d. Pure binary
e. All of the above

___ 9. Which is not a characteristic of parallel data transmission?

a. Faster
b. Requires more hardware
c. Requires less hardware
d. All of the above
e. None of the above

___ 10. Identify the odd number in the list below.

a. 10110110
b. 10111111
c. 10000000
d. 11111110
e. 11010

___ 11. What is the largest binary number that can be represented with 10 bits?

a. 255
b. 1000
c. 1023
d. 1024
e. None of the above

___ 12. How many discrete steps or states are there in a 10-bit number?

a. 255
b. 1000
c. 1023
d. 1240
e. 1024

___ 13. The decimal equivalent of the binary number 11011010 is _____ .

a. 200
b. 218
c. 222
d. 230
e. 250

___ 14. The binary equivalent of 148_{10} is _____.

a. 10010100
b. 10001010
c. 11001100
d. 10101010
e. 11001

___ 15. The octal equivalent of binary 101101100 is _____ .

a. 542
b. 433
c. 653
d. 554
e. 550

___ 16. The binary equivalent of hexadecimal FA is _____ .

a. 10010100
b. 10101111
c. 11111010
d. 10101010
e. 11001

___ 17. The hexadecimal equivalent of decimal 199 is _____ .

a. C7
b. DD
c. D7
d. D0
e. F2

___ 18. The hexadecimal equivalent of binary 10101011 is _____ .

a. AC
b. AB
c. BA
d. 1011
e. HA

___ 19. The octal equivalent of hexadecimal 9F is _____ .

a. 180
b. 255
c. 237
d. 250
e. 275

___ 20. Assuming inverted input logic, what is the decimal value represented by the voltages illustrated below? (A = LSB)

a = -5v B = 5v C = 5v D = -5v E = -5v

a. 12
b. 19
c. 25
d. 6
e. 8

NOTE: Completion of this unit test to specified score is the student's final evaluation for competencies K1 and K10.

ANSWERS TO UNIT TEST

1.	b	(K10)	11.	c	(K1)
2.	d	(K10)	12.	d	(K1)
3.	d	(K10)	13.	b	(K1)
4.	b	(K10)	14.	a	(K1)
5.	b	(K1)	15.	d	(K1)
6.	c	(K1)	16.	c	(K1)
7.	d	(K1)	17.	a	(K1)
8.	a	(K1)	18.	b	(K1)
9.	c	(K10)	19.	c	(K1)
10.	b	(K1)	20.	c	(K1)

MODULE: DIGITAL LOGIC APPLICATION

UNIT II: LOGIC GATES

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to identify logic gates by schematic symbol, Boolean expression or truth table. This knowledge will be evidenced by achieving a specified score on the unit test.

SPECIFIC OBJECTIVES

After completion of the lesson in this unit, the student should be able to:

1.1 Identify terms and definitions.

1.2 Describe characteristics of each of the two major classifications of logic circuits.

1.3 Identify the schematic symbol, Boolean expression or truth table for the following logic gates: NOT, AND, NAND, OR, NOR, XOR and XNOR. (competency K2 and K3)

1.4 Identify inverted input (negative) logic gates and state their positive logic equivalents. (competency K2)

1.5 Identify tri-state devices and describe their operation.

1.6 Breadboard digital integrated circuits. (competency K2, JS 1.1)

DIGITAL LOGIC APPLICATION

UNIT II: LOGIC GATES

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plan

1. Lesson 1: LOGIC GATES

   a. Information outline

   b. Handout

      HO 1.1: Inverted input logic gates

   c. Assignment sheet

      AS 1.1: Digital logic circuits

   d. Answers to assignment sheet

   d. Job sheet

      JS 1.1: Breadboard digital integrated circuits

E. Unit test

F. Answers to unit test

REFERENCES

A. Book

1. Digital Techniques (Book 1 and 2). Benton Harbor, MI: Heath Co., 1986.

NOTES TO THE INSTRUCTOR

A. Suggested approaches to teaching this unit

1. Orient students to trainers used to teach digital logic circuits.

2. Demonstrate how to use the TTL Logic Data Manual (Sunnyvale, Calif.: Signetics Company, 1982).

3. Introduce students to digital integrated-circuit data sheets from an I.C. manufacturer.

C. Suggested supplemental materials

1. TTL Logic Data Manual. Sunnyvale, CA: Signetics Company, 1982.

2. Logic Gates (E-89-361). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

MODULE: DIGITAL LOGIC APPLICATION

UNIT II: LOGIC GATES

LESSON 1: LOGIC GATES

I. Terms and definitions

A. Boolean expression--letters and symbols used to represent a logic gate or gate combinations

B. Gate--circuit having one or more inputs and one output. The output depends on the logic state of the input or input combinations.

C. Truth table--tabulation that illustrates the relationship between various input combinations and the resulting output

II. Types of logic circuits

A. **Decision-making** circuits are made from a combination of logic elements called gates. Therefore, decision-making circuits are classified as combinational logic circuits.

B. **Memory** circuits

1. This circuit type stores data.

2. The basic storage element is a flip-flop which can be made from a combination of logic gates.

3. Memory circuits are called sequential logic circuits when they are connected one after another.

NOTE: The three logic elements used to construct sequential and combinational circuits are the AND gate, OR gate and invertor.

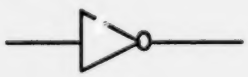
III. Logic gates

A. The inverter (NOT gate)

1. The invertor is the simplest form of digital logic.

2. The output of an invertor is always the opposite or complement of the input.

3. Schematic symbol



NOTE: The bubble always denotes inversion.

4. Truth table

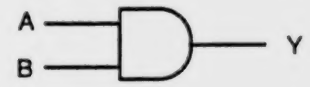
A	$\overline{Y}$
0	1
1	0

5. Boolean expression: $A = \overline{Y}$

NOTE: An invertor always has only one input and one output.

B. The AND gate

1. Has two or more inputs
2. The number of possible input combinations can be found by using the following formula: # of input combinations = 2^N.
3. The only time that there is a high at the output is when <u>all</u> inputs are high.
4. Schematic symbol



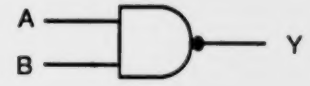
5. Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

6. Boolean expression: A x B = Y

C. The NAND gate

1. The NAND gate is simply an AND gate that has an inverted output.
2. Schematic symbol



3. Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

4. Boolean expression: $\overline{A \times B} = Y$

D. The OR gate

1. Has two or more inputs
2. Has an output high if any <u>one</u> input is high
3. Schematic symbol

4. Sometimes referred to as an inclusive OR

5. Truth table

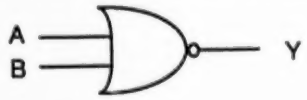
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

6. Boolean expression: $A + B = Y$

E. The NOR gate

1. The NOR gate is simply an OR gate that has the output inverted.

2. Schematic symbol



3. Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

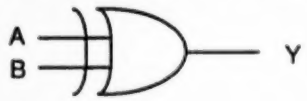
4. Boolean expression: $\overline{A + B} = Y$

F. The XOR gate

1. The XOR gate is referred to as the exclusive OR gate.

2. The XOR gate will have a high at the output when an odd number of highs are present at the inputs.

3. Schematic symbol



4. Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

5. Boolean expression: $A \oplus B = Y$

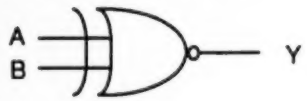
G. The XNOR gate

1. Commonly referred to as the exclusive NOR gate

2. The XNOR gate is the same as an XOR gate except that it has an invertor at the output.

3. The XNOR gate will output a low when there are an odd number of highs at the input.

4. Schematic symbol



5. Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

6. Boolean expression: $\overline{A \odot B} = Y$

IV. Positive and inverted input logic gates (HO 1.1)

A. Positive logic gates include all of the gates discussed up to this point.

B. Inverted input (negative) logic gates

1. Inverted input logic gates have invertors preceding the inputs.

2. After reviewing the truth tables for inverted input AND, NAND, OR and NOR gates, notice that an inverted NAND has the same truth table as a positive NOR gate.

Positive AND = Inverted OR
Positive OR = Inverted AND
Positive NAND = Inverted NOR
Positive NOR = Inverted NAND

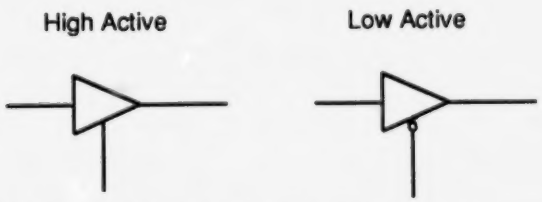
V. Tri-state logic

A. Tri-state logic or three-state logic has the normal low- or high-output states plus a high impedance or floating-output state which allows the circuit to "disappear" when not enabled.

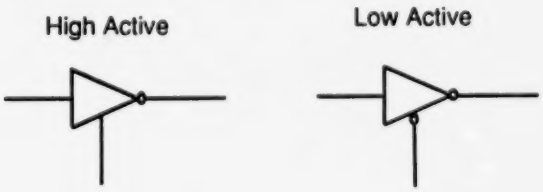
NOTE: An external pin tied to the gate applies either an active high or active low input to enable or disable the logic gate.

B. Tri-state buffers

1. Non-inverting buffers do not invert the input, but the buffer produces more current and increases the number of loads on the output (fan-out).

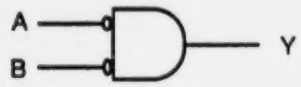


2. Inverting buffers invert the input as well as produce an increase in current, which allows an increase in the number of loads.



INVERTED INPUT LOGIC GATES

Inverted input AND

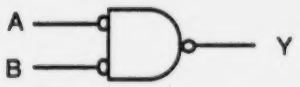


$\overline{A} \times \overline{B} = Y$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(same as positive NOR)

Inverted input NAND



$\overline{\overline{A} \times \overline{B}} = Y$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(same as positive OR)

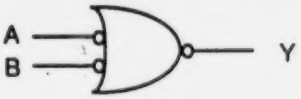
Inverted input OR

$\overline{A} + \overline{B} = Y$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(same as positive NAND)

Negative NOR



$\overline{\overline{A} + \overline{B}} = Y$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(same as positive AND)

DIGITAL LOGIC CIRCUITS

Write the truth table, Boolean expression and schematic symbol for each of the following gates.

1. AND gate

Symbol:

A	B	Y
0	0	
0	1	
1	0	
1	1	

Boolean expression:

2. NAND gate

Symbol:

A	B	Y
0	0	
0	1	
1	0	
1	1	

Boolean expression:

3. Inverter gate

Symbol:

A	Y
0	
1	

Boolean expression:

4. OR gate

Symbol:

A	B	Y
0	0	
0	1	
1	0	
1	1	

Boolean expression:

5. NOR gate

Symbol:

A	B	Y
0	0	
0	1	
1	0	
1	1	

Boolean expression:

6. XOR gate

Symbol:

A	B	Y
0	0	
0	1	
1	0	
1	1	

Boolean expression:

7. XNOR gate

Symbol:

A	B	Y
0	0	
0	1	
1	0	
1	1	

Boolean expression:

8. Logic circuits can be classified into two distinct categories: _____ and _____.

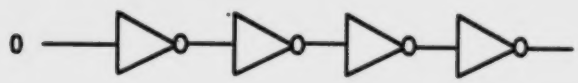
9. What does inverted input logic mean?

10. An AND gate has six inputs.

    a. How many input combinations are possible? _____

    b. How many times will the output be 1? _____

11. What is the output of the following logic circuits?



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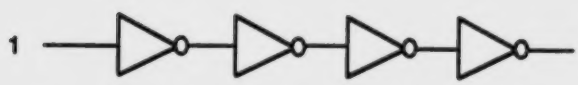

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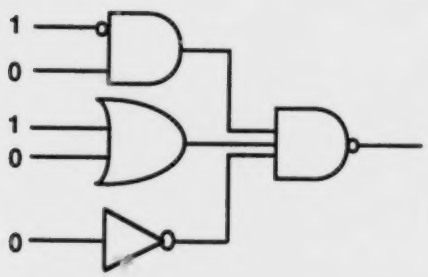


_____

12. Complete the following.

+ AND = - _____

+ OR = - _____

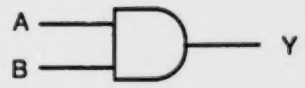
+ NAND = - _____

+ NOR = - _____

ANSWERS TO AS 1.1

1. AND gate

Symbol:



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Boolean expression:

$A \times B = Y$

2. NAND gate

Symbol:

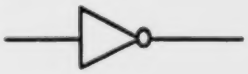
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Boolean expression:

$\overline{A \times B} = Y$

3. Inverter gate

Symbol:



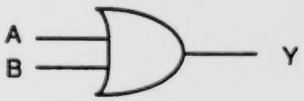
A	Y
0	1
1	0

Boolean expression:

$A = \overline{A}$

4. OR gate

Symbol:



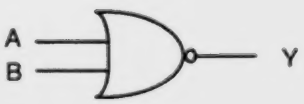
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Boolean expression:

$A + B = Y$

5. NOR gate

Symbol:



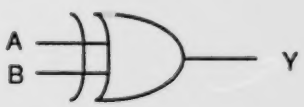
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Boolean expression:

$\overline{A + B} = Y$

6. XOR gate

Symbol:



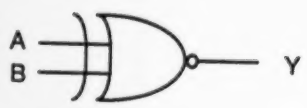
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Boolean expression:

$A \oplus B = Y$

7. XNOR gate

Symbol:



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Boolean expression:

$\overline{A \oplus B} = Y$

8. Memory, decision-making

9. Inputs are inverted preceding logic gates.

10. 64, 1

11. 0, 0, 1

12. OR, AND, NOR, NAND

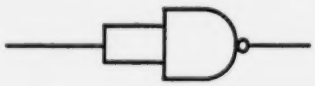
BREADBOARD DIGITAL INTEGRATED CIRCUITS

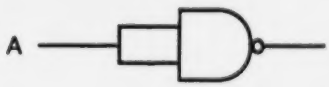
Equipment:

Digital trainer
7400 NAND gate
TTL Logic Data Manual

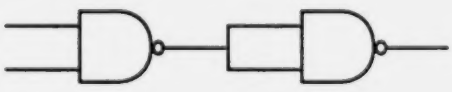
Procedure:

		Evaluation 3	2	1	N
1.	Use the TTL Logic Data Manual to find the pin configuration of the 7400 I.C. Draw the pin configuration of the I.C. below.	—	—	—	—
2.	Place the 7400 I.C. on the breadboard and connect the pin labeled V_{cc} to five volts and the pin labeled GND to ground.	—	—	—	—
3.	Tie two input pins of one NAND gate together as illustrated. Input a logic 1 at this point.	—	—	—	—
4.	Monitor the output of the gate. With the input as a logic 1, the output of the gate is a logic _____ .	—	—	—	—
5.	Now change the input to a logic low. With a logic low at the input, the output is a logic _____ .	—	—	—	—
6.	Develop a truth table for the gate below. Call the input A and the output Y.	—	—	—	—
7.	When the inputs of a NAND gate are tied together, the gate behaves like an _____ .	—	—	—	—
8.	If this combination were placed at the output of a NAND gate as shown below, a _____ gate would result.	—	—	—	—

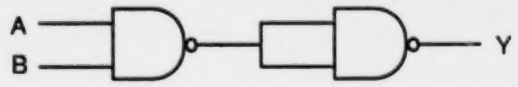




A Y



9. Connect the pins of the 7400 so that the following circuit is constructed. — — — —



10. Complete the truth table below for the logic circuit just constructed. — — — —

A	B	Y
0	0	
0	1	
1	0	
1	1	

11. This circuit behaves like a _____ gate. — — — —

12. Based on knowledge gained from steps 1 through 11: — — — —

    a. What type of gate would the combination of NAND gates below create?

    b. True or false? A combination of NAND gates can be constructed to create a NOT, OR, NOR, AND or NAND gate.

Average of above evaluations* — — — —

*This average is the student's final evaluation for competency K2: Identify and describe the operation of basic logic gates.

MODULE: DIGITAL LOGIC APPLICATION

UNIT II: LOGIC GATES

UNIT TEST

Choose the option which best answers the question or completes the statement.

____ 1. The two distinct classifications of logic circuits are _____.

a. Microprocessor
b. Decision-making
c. Memory
d. Parallel
e. Combinational

____ 2. Which type of logic gate complements the input bit?

a. NOT
b. AND
c. NAND
d. OR
e. None of the above

____ 3. Which type of logic gate will produce a high at the output only when all input bits are high?

a. NOT
b. AND
c. NAND
d. OR
e. None of the above

____ 4. Which type of logic gate will produce a low at the output only when all input bits are high?

a. NOT
b. AND
c. NAND
d. OR
e. None of the above

____ 5. Which type of logic gate will produce a low at the output when any or both input bits are high?

a. AND
b. NAND
c. NOR
d. OR
e. None of the above

____ 6. The Boolean expression A + B = Y is for which kind of gate?

a. AND
b. NAND
c. NOR
d. OR
e. None of the above

____ 7. The Boolean expression $\overline{A \times B}$ = Y is for which kind of gate?

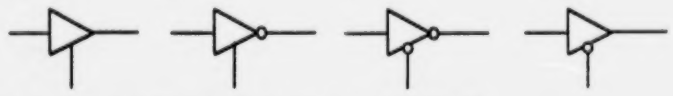
a. AND
b. NAND
c. NOR
d. OR
e. None of the above

____ 8. An inverted NAND gate equals a positive _____.

a. AND
b. NAND
c. NOR
d. OR
e. None of the above

___ 9. Which of the following schematic symbols is the symbol for a low active non-inverting buffer?

A. B. C. D.



___ 10. Which of the following appropriately describes a gate?

a. Letters and symbols used to represent a logic gate or gate combinations
b. Circuit having one or more inputs and one output
c. Tabulation that illustrates the relationship between various input combinations and the resulting output
d. Circuit having one or more outputs and one input
e. None of the above

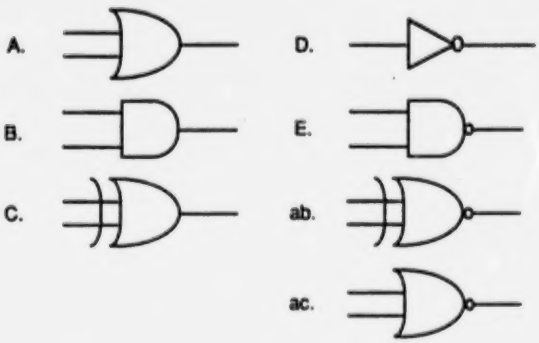
___ 11. How do tri-state buffers act when the circuit is inhibited?

a. Output is binary 1
b. Output is binary 0
c. Circuit seems to disappear
d. Circuit appears as a short
e. None of the above

Match each schematic symbol to the appropriate gate.

___ 12. NAND
___ 13. AND
___ 14. NOR
___ 15. OR
___ 16. NOT
___ 17. XOR
___ 18. XNOR

A. B. C. D. E. ab. ac.



Use the <u>TTL Logic Data Manual</u> to find the 7400 series number for AND, OR, NOR and NOT gates.

___ 19. AND:
___ 20. OR:
___ 21. NOR:
___ 22. NOT:

ANSWERS TO UNIT TEST

1. b, c
2. a (K2)
3. b (K2)
4. c (K2)
5. c (K2)
6. d (K2)
7. b (K2)
8. c (K2)
9. d (K2)
10. b (K2)
11. c (K2)
12. e (K2)
13. b (K2)
14. ac (K2)
15. a (K2)
16. d (K2)
17. c (K2)
18. ab (K2)

19-22. To be evaluated by instructor (K2)

MODULE: DIGITAL LOGIC APPLICATION

UNIT III: DIGITAL INTEGRATED CIRCUITS

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to use manufacturer sources such as the TTL Logic Data Manual to determine digital integrated circuit (I.C.) specifications and to identify digital I.C. families and characteristics. This knowledge will be evidenced by achieving a specified score on the unit test.

SPECIFIC OBJECTIVES

After completion of the lesson in this unit, the student should be able to:

1.1 Identify acronyms related to digital I.C.s.

1.2 Explain terminology as it relates it to digital integrated circuit characteristics.

1.3 Identify characteristics of integrated circuit packages. (competency K5)

2.1 Identify TTL families of digital I.C.s by numbers and characteristics.

2.2 Identify CMOS families of digital I.C.s by numbers and characteristics.

DIGITAL LOGIC APPLICATION

UNIT III: DIGITAL INTEGRATED CIRCUITS

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plans

1. Lesson 1: DIGITAL I.C. CHARACTERISTICS

   a. Information outline

   b. Assignment sheet

      AS 1.1: Introduction to digital I.C.s
      AS 1.2: Using TTL Logic Data Manual

   c. Answers to assignment sheets

2. Lesson 2: DIGITAL LOGIC FAMILIES

   a. Information outline

   b. Assignment sheet

      AS 2.1: Digital logic families

   c. Answers to assignment sheet

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. Digital Techniques (Book 1 and 2). Benton Harbor, MI: Heath Co., 1986.

2. TTL Logic Data Manual. Sunnyvale, CA: Signetics Company, 1982.

NOTES TO THE INSTRUCTOR

A. Suggested approaches to teaching this unit

1. For Lesson 2, refer to the TTL Logic Data Manual, General Index or other manufacturer sources for data sheet information to illustrate TTL and CMOS families in more depth.

B. Suggested supplemental material

1. Logic Families (E-89-362) (1/2" video). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

2. TTL Logic Data Manual. Sunnyvale, CA: Signetics Company, 1982.

MODULE: DIGITAL LOGIC APPLICATION

UNIT III: DIGITAL INTEGRATED CIRCUITS

LESSON 1: DIGITAL I.C. CHARACTERISTICS

I. Acronyms and abbreviations

A. CMOS--complementary metal-oxide field-effect transistor

B. DIP--dual in-line package

C. DVM--digital volt meter

D. ECL--emitter-coupled logic

E. FET--field-effect transistor

F. I.C.--integrated circuits

G. IIL--integrated injection logic

H. LSI--large-scale integration

I. MOS device--semiconductor component constructed by metal-oxide semiconductor process. Current can flow in either of two directions.

J. MOSFET--metal-oxide field-effect transistor

K. MSI--medium-scale integration

L. NMOS--opposite of PMOS; MOS devices made on P-type silicon supporting material; 2-3 times faster than PMOS

M. ns--nanoseconds

N. PMOS--opposite of NMOS; MOS devices made on P-type silicon supporting material; has a predominantly positive charge

O. SSI--small-scale integration

P. TTL--transistor-transistor logic

Q. VLSI--very large-scale integration

II. Digital I.C. characteristics

A. Logic levels

1. Logic levels are the voltage levels assigned to a binary 1 and binary 0.

2. Most manufacturers specify maximum and minimum acceptable values by using the following expressions.

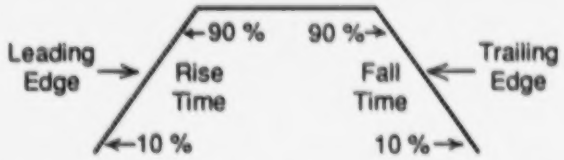
a. V_{IH}^{MIN}--minimum voltage level allowable for a logic 1 at an input

b. V_{IL}^{MAX}--maximum voltage level allowable for a logic 0 at an input

c. V_{OH}^{MIN}--minimum voltage level acceptable for a logic 1 at an output

d. V_{OL}^{MAX}--maximum voltage level acceptable for a logic 0 at an output

3. Leading edge vs. trailing edge



a. Rise time of an input or output pulse--time required for a pulse to rise from 10% to 90% of maximum value

b. Fall time of an input or output pulse--time required for a pulse to fall from 90% to 10% of maximum value

B. Propagation delay--time between application of an input pulse and the corresponding output change

1. Speed of operation is one of the most important characteristics of most digital circuits.

2. High speed is desirable for most applications.

C. Power dissipation--supply power consumed by a logic circuit

1. Usually measured or calculated under the worst case conditions when the integrated circuit is under maximum load

2. Calculated by the following formula: $P_D = I_{IC} \times V_{IC}$

3. The total power dissipated by all integrated circuits determine the size and cost of the power supply.

D. Power-speed tradeoff--relationship between the integrated circuit's power consumption and propagation delay time

1. Usually, if the I.C. is faster, the power dissipation is greater; if the power dissipation is less, the speed is slower.

2. Integrated circuits made from bipolar transistors are faster but consume greater amounts of power than the MOSFET counterparts.

3. Integrated circuits made from MOSFETs consume less power but have a slower processing speed.

E. Noise immunity

1. Stray electrical and magnetic fields can produce noise pulses on inputs and outputs of logic circuits.

2. Noise immunity refers to the logic circuit's ability to tolerate this noise.

F. Fan out

1. Fan out of an integrated circuit specifies how much load (number of gates) that can be connected to a logic circuit output before excessive loading occurs.

2. Example: A fan out of 10 indicates that 10 separate logic gate inputs can be placed at the output while still maintaining proper operation.

G. Classifications of integrated circuits

1. According to manufacturing method

a. Thin/thick film

b. Monolithic

c. Hybrid

2. According to function

a. Small-scale integration (SSI) chips contain simple logic gates or flip-flops.

b. Medium-scale integration (MSI) chips contain gates combined to form complete circuits such as counters, dividers, registers, etc.

c. Large-scale integration (LSI) chips contain complete circuits that form a complete system such as the I.C.s found in DVMs, calculators and the microprocessors found in today's personal computers.

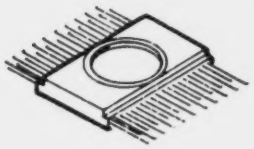
d. Very large-scale integration (VLSI) chips contain gates and circuits combined to form complete systems (as with LSI chips) but are typically associated with the super mainframe computer systems.

III. Integrated circuit packages

A. TO5 (transistor outline)

1. Earliest integrated circuit package

2. Still available for some I.C. types but is not widely used

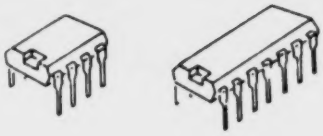


B. Flat pack

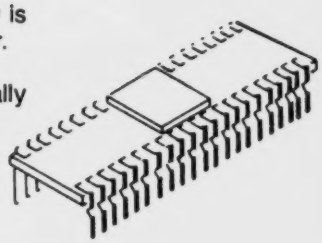
1. Increasingly popular package

2. Used where space is of the utmost importance

C. DIP (dual in-line package)



1. Most popular integrated circuit package
2. Comes in two varieties: plastic and ceramic. The ceramic variety is used in applications in which the I.C. may need to dissipate power.
3. Comes in a variety of sizes. The 14, 16, 18, 20 and 40 are generally the most popular.
4. Counting the pin numbers on the DIP
   a. Find a notch or dot on the integrated circuit.
   b. With the notch or dot to the left, the pin below the notch or dot is pin number 1.
   c. Count in a counter-clockwise direction.



INTRODUCTION TO DIGITAL I.C.s

1. Draw a digital signal. Indicate the leading and trailing edge of the waveform.

Define the following terms.

2. Propagation delay:

3. Power dissipation:

4. Power-speed tradeoff:

5. Noise immunity:

6. Fan out:

7. List four classifications of digital I.C.s.

   a.

   b.

   c.

   d.

USING TTL LOGIC DATA MANUAL

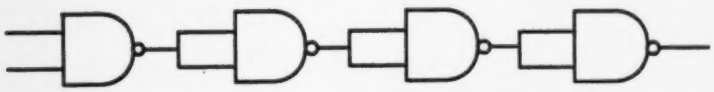
Use a TTL Logic Data Manual to find the specifications of the following digital integrated circuits.

	Type	Propagation delay/F_{MAX}	Fan out	Power dissipation
1. 7400				
2. 74LS00				
3. 7404				
4. 74LS04				
5. 74192				
6. 74LS192				
7. 7474				
8. 74LS74				

9. Under worst-case conditions, what is the minimum power delivery of the power supply for a logic circuit containing the following digital I.C.s? _____

   1 - 7400
   2 - 74LS04
   2 - 7474
   1 - 7410
   2 - 74LS90

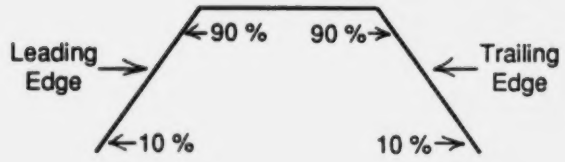
10. The four logic gates within a 7400 are cascaded as illustrated below. What is the total propagation delay of the circuit? _____



NOTE: Completion of this assignment sheet to specified score is the student's partial evaluation for competency K11: Use data sheets.

ANSWERS TO AS 1.1

1.



2. Propagation delay: time between application of an input pulse and the corresponding output change

3. Power dissipation: supply power consumed by a logic circuit

4. Power-speed tradeoff: relationship between the integrated circuit's power consumption and propagation delay time

5. Noise immunity: ability of a logic circuit to tolerate stray electrical and magnetic fields

6. Fan out: number of gates that can be connected to a logic circuit output before excessive loading occurs

7. TTL, MOS, ECL, IIL

ANSWERS TO AS 1.2

		Type	Propagation delay/F_{MAX}	Fan out	Power dissipation
1.	7400	Quad 2 input NAND gate	9 ns	10	40mW
2.	74LS00	Quad 2 input NAND gate	9.5 ns	10	8mW
3.	7404	Hex inverter	10 ns	10	60mW
4.	74LS04	Hex inverter	9.5 ns	10	12mW
5.	74192	Presettable BCD up/down counter	32 MHz	10	325mW
6.	74LS192	Presettable BCD up/down counter	32 MHz	10	95mW
7.	7474	Dual D type flip-flop	25 MHz	10	85mW
8.	74LS74	Dual D type flip-flop	3 MHz	10	20mW

9. 354mW

10. 36 ns

MODULE: DIGITAL LOGIC APPLICATION

UNIT III: DIGITAL INTEGRATED CIRCUITS

LESSON 2: DIGITAL LOGIC FAMILIES

NOTE: Many more types of logic families have been and are being developed. Consult suppliers (such as Texas Instruments) for up-to-date indexes on types, identification and characteristics.

I. TTL (transistor-transistor logic)

A. Uses bipolar transistors to implement logic gates

B. Most widely used type of logic family due to its low cost, availability and high performance

C. Most common: the 7400 series marketed by Texas Instruments. Other TTL circuits are the 9300 series from Fairchild and the series manufactured by Signetics. All of these are compatible with each other.

1. A military grade of 7400 series I.C.s, which have improved specifications, are available. These I.C.s are labeled with the 5400 series.

2. Many standard TTL numbers are preceded by letters. Examples: SN7400 or SN74LS00 (low-power Schottky)

D. In many cases devices may be interchanged, providing the following considerations are met.

1. Devices must be pin-compatible.

2. Supply voltage for TTL devices cannot exceed ±5 volts.

3. The speed at which a device is operated at must be within the circuit's design limits. (Ex.: clock speed)

4. Power consumption should be considered. For example, the TTL is less desirable for battery-operated circuits.

5. Fan out (the number of devices driven) must be considered.

E. Typical TTL values

1. Propagation delay: 1-50 nanoseconds

2. . Fan out: 20-30

3. Noise immunity: good

4. Logic levels: 0.4 volts = binary 0
3.6 volts = binary 1

5. Supply voltage: 5 volts

II. TTL variations

A. Low-power TTL (74Lxx)

1. The tradeoff for less power consumption is a longer propagation delay.

2. This variation uses approximately one-tenth the power of a standard TTL.

3. Generally, the low-power TTL I.C.s are being replaced by the low-power Schottky.

B. High-speed TTLs (74Hxx)

1. This type, which utilizes extra transistors, sacrifices power consumption for lower propagation delays.

2. Generally, these TTLs are also being replaced by the superior Schottky TTL.

C. Schottky TTL (74Sxx)

1. Propagation delays of 3 nanoseconds (ns) are possible with a power consumption less than that used by a high-power TTL.

2. These logic gates, constructed from transistors using Schottky (metal-silicon) diodes, prevent saturation and allow faster switching speeds.

3. Because high-speed circuits such as Schottky and ECL generate very sharp wave fronts that cause transmission and coupling, it is unwise to use these circuits except where high speed is essential to the application.

D. Low-power Schottky (74LSxx)

1. Formed by using Schottky diodes to speed up the TTL circuit, then raising the values of internal resistors, which increases the delay

2. Speed approximately equal to a standard TTL

3. Consumes only about one-fifth the power of a standard TTL gate because of high resistances

E. Advanced low-power Schottky (74ALSxx/74ASxx)

1. Utilizes an advanced wafer fabrication process

2. Less subject to noise

3. Can tolerate 10% voltage variations in the power supply

4. Offers the high-speed operation desirable in most digital applications

III. Emitter-coupled logic (ECL) circuit

A. This type is one of the fastest logic circuits available.

B. A greater power consumption makes them unacceptable for most applications, however.

C. The most widely used ECLs are Motorola's MECL and 10K series.

D. Typical ECL values

1. Propagation delay: 0.5-3 nanoseconds

2. Fan out: 10-25

3. Noise immunity: good

4. Logic levels: -1.75 volts = binary 0
   -0.9 volts = binary 1

5. Supply voltage: -5.2 volts

IV. Metal-oxide field-effect transistor (MOSFET)

A. Advantages of MOSFET use to create the logic gates: less space, higher density chips, high input impedance and low power consumption

B. Tradeoff of MOSFET use: much slower switching speeds than can be achieved with TTL or ECL

C. Varieties

1. NMOS FETs--constructed entirely from N channel FETs

2. PMOS FETs--constructed entirely from P channel FETs

3. CMOS (complementary metal-oxide field-effect transistor)--constructed from PMOS and NMOS (complementary) devices

D. Typical MOS and CMOS values

1. Propagation delay: MOS: 50-300 ns
   CMOS: 70 ns

2. Fan out: MOS: 20-50
   CMOS: 50

3. Noise immunity: MOS: good
   CMOS: very good

4. Logic levels: 0v = binary 0
   V_{DD} = binary 1

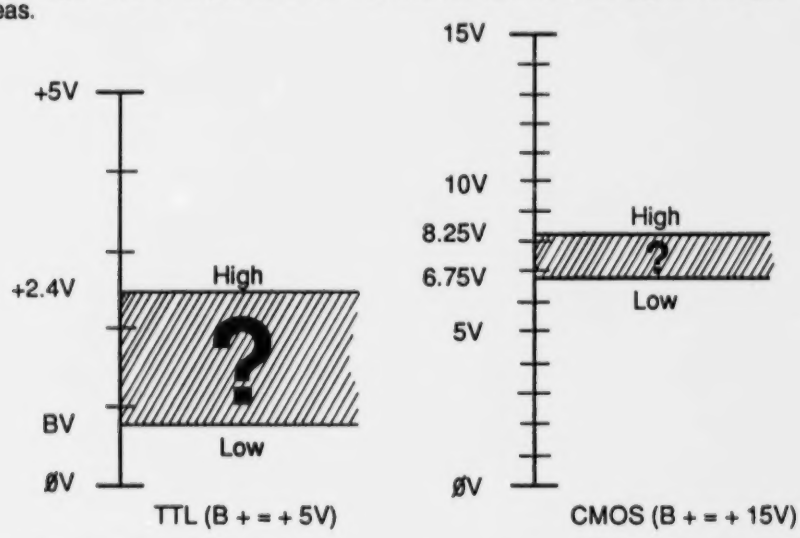
5. Supply voltage: 3-15 volts

E. CMOS gates are available from RCA under a 4000 series, and CMOS versions of the 7400 series are made by National Semiconductor under a 74C00 number series.

F. Although they are not TTL, CMOS I.C.s are generally pin-for-pin compatible with Texas Instrument's 7400 TTL series.

G. Handling precautions should be observed with all MOS and CMOS devices to avoid any static discharge.

H. Typical TTL and CMOS logic levels are shown below. When voltage falls into the areas marked with a ?, the logic level is unpredictable. For this reason, keep all signal voltages in the high or low areas.



V. Integrated injection logic (IIL)

A. Newest form of digital integrated circuits

B. Designed to combine the fast switching speeds of bipolar devices with the small size of MOS devices (only occupies half the space of MOS devices). The result is a high-speed, high-density chip.

C. Power consumption is slightly higher than that of CMOS gates.

D. IIL has the best power-speed tradeoff available.

DIGITAL LOGIC FAMILIES

Fill in the following table showing the typical specifications of the four logic families.

	TTL	ECL	MOS
1. Propagation delay			
2. Fan out			
3. Noise immunity			
4. Logic levels			
5. Supply voltage			
6. Power consumption			

7. List three considerations for interchanging devices.

   a.

   b.

   c.

ANSWERS TO AS 2.1

		TTL	ECL	MOS
1.	Propagation delay	1-50 ns	.5-3 ns	50-30 ns
2.	Fan out	20-30	10-25	20-50
3.	Noise immunity	good	good	good to very good
4.	Logic levels	.4v = binary 0 3.6 = binary 1	-1.75 = binary 0 -.9 = binary 1	0v = binary 0 V_{DD} = binary 1
5.	Supply voltage	5v	-5.2v	3-15v
6.	Power consumption	low to medium	high	low

7. Any three of the following:
   a. Devices must be pin-compatible.
   b. Supply voltage for TTL devices cannot exceed ±5 volts.
   c. The speed at which a device is operated
   d. Power consumption
   e. Fan out

MODULE: DIGITAL LOGIC APPLICATION

UNIT III: DIGITAL INTEGRATED CIRCUITS

UNIT TEST

Select the option which best answers the question or completes the statement.

___ 1. The specification V_{OH}^{MIN} is the _____ voltage level acceptable for a logic _____ input.

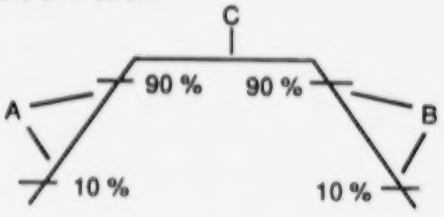
a. Minimum, 1
b. Maximum, 0
c. Minimum, 0
d. Maximum, 1
e. Minimum, 2

___ 2. The specification V_{IL}^{MAX} is the _____ voltage level acceptable for a logic _____ input.

a. Minimum, 1
b. Maximum, 0
c. Minimum, 0
d. Maximum, 1
e. Minimum, 2

___ 3. Identify the leading edge and trailing edge of the waveform below.

a. A is the leading edge
b. A is the trailing edge
c. B is the leading edge
d. C is the trailing edge
e. C is the leading edge



___ 4. Rise time can be referred to as time required for _____ .

a. An output to rise from logic input
b. An integrated circuit to respond to an input
c. A pulse to change from 90% to 10% of maximum
d. A pulse to change from 10% to 90% of maximum
e. None of the above

___ 5. Power dissipation is usually calculated under _____ conditions or when the integrated circuit is under _____ load conditions.

a. Worst case, maximum
b. Best case, maximum
c. Worst case, minimum
d. Best case, minimum
e. Normal, minimum

___ 6. The digital I.C. family with the best power-speed tradeoff is _____ .

a. TTL
b. ECL
c. MOS
d. IIL
e. CMOS

___ 7. Of the devices listed below, which has the best fan out?

a. TTL
b. ECL
c. MOS
d. IIL
e. CMOS

___ 8. Which of the following devices are static-sensitive?

a. TTL
b. MOS
c. CMOS
d. Both b and c
e. All of the above

___ 9. Which of the following is <u>not</u> a TTL variation?

a. 74S00
b. 74L00
c. 74P00
d. 74C00
e. All of the above

___ 10. Which of the following integrated circuit classifications contains gates and flip-flops?

a. SSI
b. MSI
c. LSI
d. VLSI
e. None of the above

___ 11. Which of the following I.C. classifications contain complete circuits such as counters, registers, dividers, etc.?

a. SSI
b. MSI
c. LSI
d. VLSI
e. None of the above

___ 12. Pin-for-pin compatible CMOS integrated circuits are available for the _____ series integrated circuits.

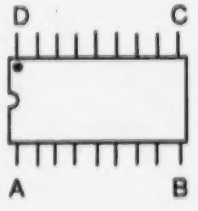
a. 74CMxx
b. 74xx
c. 74Hxx
d. 74Cxx
e. 84xx

___ 13. Which integrated circuit family would be best suited in the design of a portable battery-operated computer system?

a. TTL
b. MOS
c. ECL
d. High-speed TTL
e. None of the above

___ 14. Which point in the illustration below is pin 1?

a. A
b. B
c. C
d. D
e. None of the above



Give the spelled-out meanings for the following acronyms.

15. I.C.:

16. MOSFET:

17. DVM:

18. DIP:

19. LSI:

20. TTL:

ANSWERS TO UNIT TEST (K5)

1. a
2. b
3. a
4. d
5. a
6. d
7. e
8. d
9. d
10. a
11. b
12. b
13. b
14. d
15. Integrated circuit
16. Metal-oxide field-effect transistor
17. Digital volt meter
18. Dual in-line package
19. Large-scale integration
20. Transistor-transistor logic

DIGITAL LOGIC APPLICATION
UNIT IV: COMBINATIONAL LOGIC

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to interpret a Boolean statement for a combinational logic circuit, reduce the equation to its simplest form and design the circuit for the Boolean statement. This knowledge will be evidenced by completing the job sheet and unit test to the specified score.

SPECIFIC OBJECTIVES

After completion of the lessons in this unit, the student should be able to:

1.1 Identify terms and definitions.

1.2 Develop Boolean equations for combinational logic circuits. (competency K7)

2.1 Use Boolean algebraic laws to simplify logic circuits. (competency K7)

2.2 Design and construct a logic circuit using Boolean algebra. (competencies K3 and K7)

DIGITAL LOGIC APPLICATION

UNIT IV: COMBINATIONAL LOGIC

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plans

1. Lesson 1: BOOLEAN EQUATIONS FOR COMBINATIONAL LOGIC CIRCUITS

   a. Information outline

   b. Assignment sheet

      AS 1.1: Boolean equations

   c. Answers to assignment sheet

2. Lesson 2: SIMPLIFYING LOGIC CIRCUITS

   a. Information outline

   b. Assignment sheet

      AS 2.1: Using Boolean algebra to simplify logic circuits

   c. Answers to assignment sheet

   d. Job sheet

      JS 2.1: Design and construct a logic circuit using Boolean algebra

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. Kleitz, William. Digital Electronics, A Practical Approach. Englewood Cliffs, NJ: Prentice-Hall, 1987.

2. Tokheim, Roger L. Digital Electronics. 2nd ed. New York: McGraw-Hill, 1984.

NOTES TO THE INSTRUCTOR

A. Suggested approaches to teaching this unit

1. AS 2.1 can be further explained using Karnaugh mapping to reduce a combinational logic circuit to its simplest form.

2. JS 2.1 can be expanded by giving additional electronic combinational circuit problems. This type of exercise assists students in understanding encoders, decoders, multiplexer and demultiplexer circuits.

DIGITAL LOGIC APPLICATION

UNIT IV: COMBINATIONAL LOGIC

LESSON 1: BOOLEAN EQUATIONS FOR COMBINATIONAL LOGIC CIRCUITS

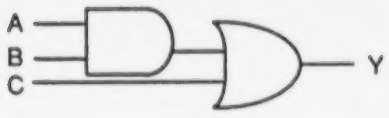
I. Terms and definitions

A. Boolean algebra--branch of mathematics used in the development of digital circuits

B. Combinational logic circuit--any circuit that accepts binary inputs and generates new binary outputs using a combination of gates and inverters

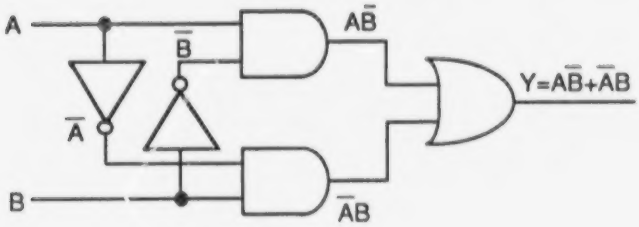
II. Design specifications

A. Combinational logic circuits use two or more logic gates to form a complex function. Shown below is a three-input combinational logic circuit made up of one AND gate and one OR gate. The truth table shows the input and output results for all combinations of inputs.



------Inputs------			Output
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

B. One of the most frequently used combinational circuits is the exclusive-OR (XOR) circuit. This combinational circuit generates a binary 1 output if either one, but not both, of its two outputs is a binary 1. Shown below are the basic circuit and truth table for an exclusive-OR gate.



--Inputs--		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

C. By using the truth table for the XOR gate, a Boolean expression can be obtained. The procedures for finding the Boolean equation for logic circuits are as follows.

1. Look at the output column of the truth table. Identify the input combinations for binary outputs. Binary 1s appear at two different locations--where A = 0 and B = 1, and where A = 1 and B = 0.

2. Write the Boolean expression for the first input combination. If A = 0, write $\overline{A}$. If B = 1, write B. Since these inputs feed an AND gate, ANDing the two terms becomes $\overline{A}B$.

3. Write the Boolean expression for the second input combination. A = 1, B = 0, and these terms ANDed together becomes AB.

4. Since the two outputs of the AND gates are applied to an OR gate, OR the two results from the AND gates, which becomes

$$\underset{\text{(output)}}{Y} = \underset{\text{(inputs)}}{\bar{A}B + A\bar{B}}$$

D. Combining gates in combinational logic circuits from Boolean expressions is a necessary skill for the technician. Combinational logic is used to design logic circuits for specific applications. For example, a logic circuit for an automobile that will meet one of the following criteria would use combinational logic.

1. The alarm (Y) will activate if the headlights (A) are on and the driver's door (B) is open.

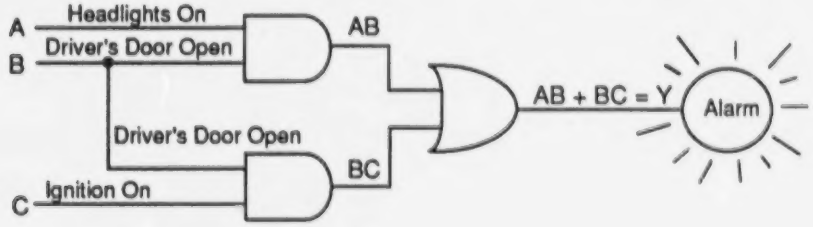
2. The driver's door (B) is open and the driver's key (C) is in the ignition.

E. The Boolean equation for the logic circuit described would be

A AND B OR C AND B = Y OR AB + CB = Y

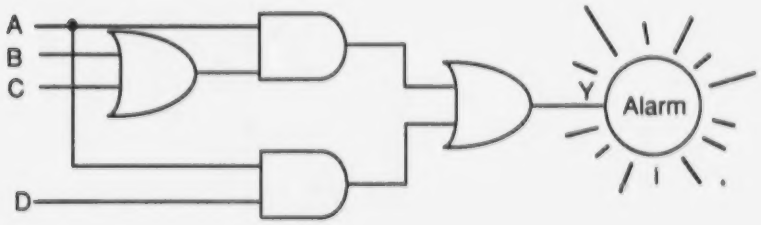
This equation states: If A AND B are at a HIGH level, OR if B AND C are at a HIGH level, then Y is at a HIGH level.

F. Put into a logic circuit, the Boolean equation AB + BC = Y would be constructed as follows.



G. Boolean equations can also be extracted from a logic circuit or the circuit can be constructed from a Boolean equation. To demonstrate this, consider the logic circuit that follows.

1. The Boolean equation for this circuit is A(B + C) + AD = Y.



2. Consider designing a logic circuit that would meet the following conditions. A store owner wants to activate an alarm (Y) if these conditions are true:

   a. If it is after 10 p.m. (A input) AND the front door (B input) OR the back door (C input) is open; OR

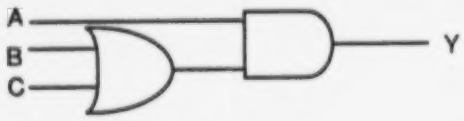
   b. If it is after 10 p.m. (A input) AND the store's safe (D input) is open

3. The circuit that would meet this criteria would be the same circuit as shown above because writing the Boolean expression becomes A(B + C) + AD = Y.

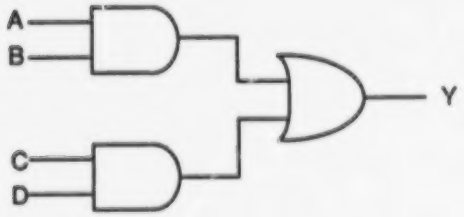
BOOLEAN EQUATIONS

Given the following combinational logic diagrams, write the Boolean equation for each to the right.

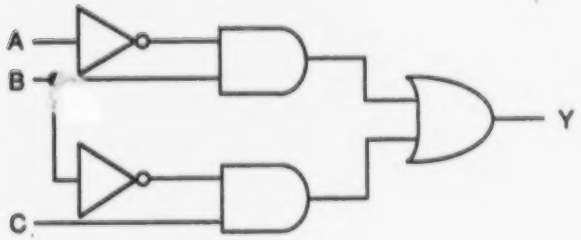
1.



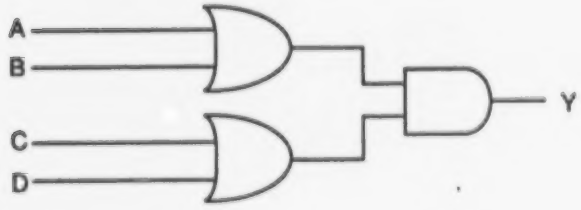
2.



3.



4.



ANSWERS TO ASSIGNMENT SHEET 1.1

1. $A(B + C) = Y$
2. $AB + CD = Y$
3. $\overline{A}B + \overline{B}C = Y$
4. $(A + B)(C + D) = Y$

DIGITAL LOGIC APPLICATION

UNIT IV: COMBINATIONAL LOGIC

LESSON 2: SIMPLIFYING LOGIC CIRCUITS

I. Boolean algebraic laws

A. Boolean algebraic laws are important for the technician to know to simplify logic circuitry, which can result in saved space, fewer integrated circuits and reduced cost.

B. There are three Boolean laws: the commutative law of addition and multiplication, the associative law of addition and multiplication, and the distributive law for expanding an equation containing ORs and AND.

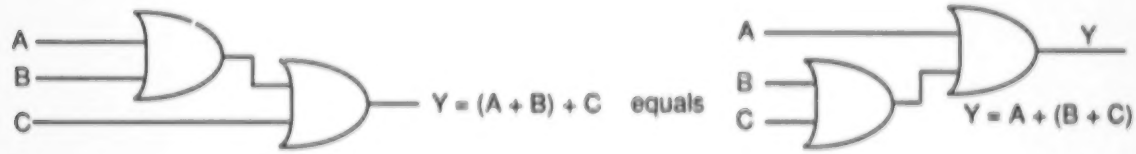
C. The commutative law of addition and multiplication states that the order of ORing and ANDing does not matter.

1. Addition

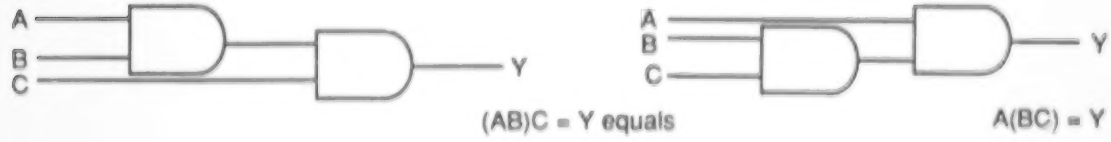
2. Multiplication

D. The associative law of addition and multiplication states that the ways variables are ORed and ANDed together does not matter.

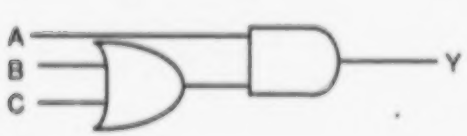
1. Addition



2. Multiplication



E. The distributive law shows the method for expanding an equation containing ORs and ANDs.



$Y = A(B + C)$ equals

$Y = AB + AC$

II. Boolean algebraic rules

NOTE: Rules derived from knowing the operation of basic gates increases the speed, ability and effectiveness of the technician in designing logic circuitry. The following rules apply to gates.

A. Anything ANDed with a 0 is equal to a 0. $A \cdot 0 = 0$

B. Anything ANDed with a 1 is equal to itself. $A \cdot 1 = A$

C. Anything ORed with a 0 is equal to itself. $A + 0 = A$

D. Anything ORed with a 1 is equal to 1. $A + 1 = 1$

E. Anything ANDed with itself is equal to itself. $A \cdot A = A$

F. Anything ORed with itself is equal to itself. $A + A = A$

G. Anything ANDed with its own complement equals 0. $A \cdot \overline{A} = 0$

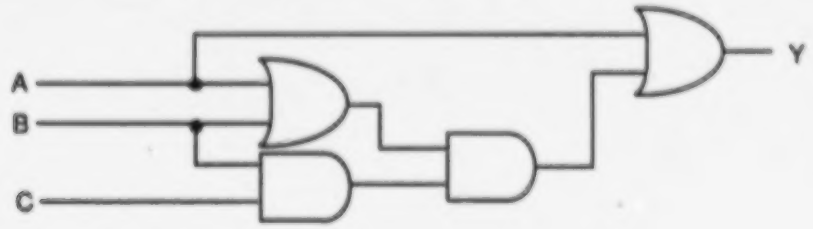
H. Anything ORed with its own complement equals 1. $A + \overline{A} = 1$

I. A variable that is complemented twice will return to its original logic level. $\overline{\overline{A}} = A$

J. $\underline{A} + \overline{A}B = \underline{A} + B$
$A + AB = A + B$

USING BOOLEAN ALGEBRA TO SIMPLIFY LOGIC CIRCUITS

Use laws and rules to simplify the logic circuit shown below. Show all work.



1. Boolean equation for Y: _____

2. Simplified Boolean equation: _____

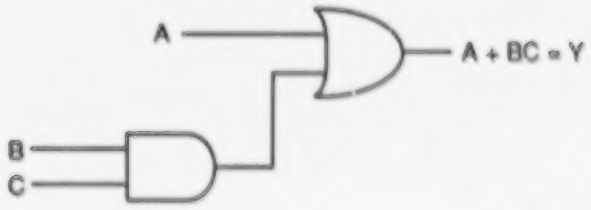
3. Draw the simplified logic circuit corresponding to the simplified Boolean equation.

ANSWERS TO ASSIGNMENT SHEET 2.1

1. $(A + B)\,BC + A = Y$

   Solution work:
   $(A + B)\,BC = ABC + BC$
   $ABC + BC + A = Y$
   $BC\,(A + 1) + A = Y$
   (Factor BC from two terms)
   $A + 1 = 1$
   $BC \times 1 + A = Y$
   $BC \times 1 = BC$
   $BC + A = Y$

2. $A + BC = Y$

3. 

DESIGN AND CONSTRUCT A LOGIC CIRCUIT USING BOOLEAN ALGEBRA

Equipment:

Solderless breadboard
DC power supply
Integrated circuits (ICs) as determined by design
LED
220Ω resistor

Specifications:

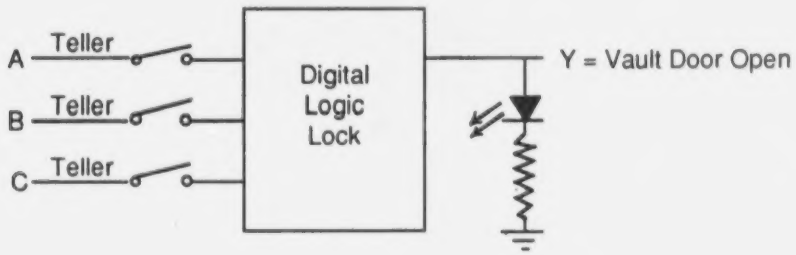
NOTE: This job sheet involves designing and constructing a logic circuit using the rules and laws of Boolean algebra. The result should include the simplest Boolean statement and the simplest logic circuit. The following conditions **must** be met by the circuit design.

1. At least two of three bank tellers (A, B and C) must close a switch to a digital lock at the same time for the bank vault door (Y) to open.

2. When a teller closes a switch, a HIGH (1, +5V) is placed on the input to the digital lock.

3. A LED with a 220Ω resistor will light if the vault door is open. It will be extinguished if the vault door is closed.

4. The diagram below represents the circuit described above.



Procedure:

	Evaluation 3	2	1	N
1. Write the Boolean statement for the circuit.	—	—	—	—
2. Write the simplest Boolean statement for the circuit.	—	—	—	—

3. Draw a logic diagram for the simplest combinational logic circuit which will meet the requirements. _ _ _ _

4. Obtain the necessary parts to wire the circuit. Wire the circuit on a solderless breadboard. _ _ _ _

5. Apply power to the circuit. Operate the circuit; record the results in the output column of the table below. _ _ _ _

Tellers Inputs			Vault door Output
A	**B**	**C**	**Y**
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

6. Does the circuit meet the requirements and expectations of the Boolean equation? YES NO _ _ _ _

7. Take down the circuit and return equipment and parts to their proper location. _ _ _ _

Average of above evaluations* _ _ _ _

*This average is the student's partial evaluation for competencies K3 and K7.

DIGITAL LOGIC APPLICATION

UNIT IV: COMBINATIONAL LOGIC

UNIT TEST

Select the option which best answers the question or completes the statement.

___ 1. Combinational logic circuits _____ .

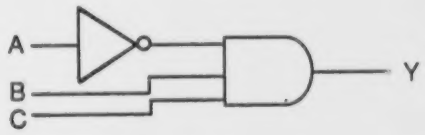
a. Use two or more logic gates
b. Have at least three inputs
c. Always use AND gates
d. Always use OR gates
e. Have one logic gate and several inputs

___ 2. Which one of the following circuits would be considered a combinational logic circuit?

a. AND
b. OR
c. NOT
d. XOR
e. XNOR

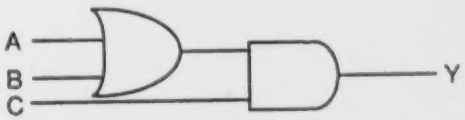
___ 3. Which of the following is the Boolean equation for the circuit below?

a. $\overline{A}BC = Y$
b. $\overline{A} + B + C = Y$
c. $\overline{ABC} = Y$
d. $\overline{A + B + C} = Y$
e. $ABC = Y$



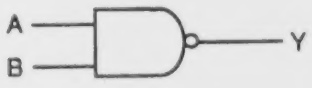
___ 4. Identify the Boolean equation for the circuit below (in its simplest form).

a. $\overline{AB} = Y$
b. $(AB) + C = Y$
c. $(A + B)\,C = Y$
d. $\overline{ABC} = Y$
e. $AB = Y$

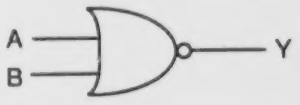


___ 5. Which of the two circuits shown below produce the same outputs?

a. A and B
b. B and C
c. A and D
d. C and D
e. A and C

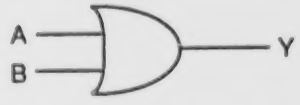


A.



B.

C.

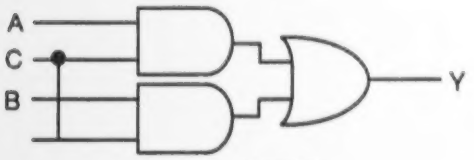


D.

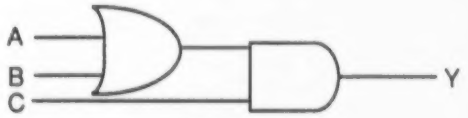
Digital 97

___ 6. Which one of the circuits below would satisfy the Boolean expression AC + BC = Y?

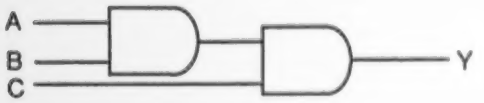
a. Circuit 1
b. Circuit 2
c. Circuit 3
d. Circuit 1 or 2
e. Circuit 1 and 3



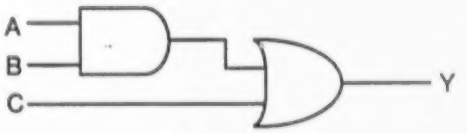
Circuit 1



Circuit 2



Circuit 3



Circuit 4

Match the gates below with their outputs using the 10 Boolean rules.

___ 7.

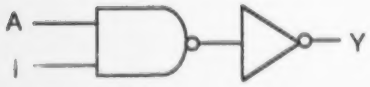
(A)

a. Y = AB
b. Y = 0
c. Y = 1

___ 8.

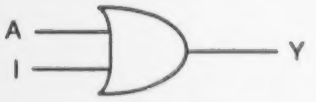
(B)

___ 9.



(C)

___ 10.



(D)

ANSWERS TO UNIT TEST (K7)

1. a
2. d
3. c
4. c
5. d
6. d
7. b
8. a
9. c
10. c

MODULE: DIGITAL LOGIC APPLICATION

UNIT V: FLIP-FLOPS

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to use flip-flops and registers in SSI and MSI form, connect flip-flops as switch debouncers, latches, storage devices and frequency dividers and determine the output of an RS, D-type or JK flip-flop. This knowledge will be evidenced by achieving a specified score on job sheets and the unit test.

SPECIFIC OBJECTIVES

After completion of the lesson in this unit, the student should be able to:

1.1 Define terminology related to flip-flops. (competency K7)

1.2 Determine the output of high-active and low-active RS flip-flops when given the input conditions. (competency K7)

1.3 Connect D-type flip-flops together to form a register. (competency K7)

1.4 Identify construction and operation aspects of JK flip-flops. (competencies K3 and K7)

1.5 Identify applications of flip-flops. (competency K7)

DIGITAL LOGIC APPLICATION

UNIT V: FLIP-FLOPS

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plan

1. Lesson 1: FLIP-FLOPS AND REGISTERS

   a. Information outline

   b. Handout

      HO 1.1: TTL Logic Data Manual excerpts

   c. Assignment sheet

      AS 1.1: Flip-flops

   d. Answers to assignment sheet

   e. Job sheets

      JS 1.1: Using an RS flip-flop
      JS 1.2: Breadboard a D-type flip-flop
      JS 1.3: Breadboard a JK flip-flop
      JS 1.4: Construct flip-flops and develop truth tables

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. Digital Techniques (Book 1 and 2). Benton Harbor, MI: Heath Co., 1986.

2. TTL Logic Data Manual. Sunnyvale, CA: Signetics Company, 1982.

NOTES TO THE INSTRUCTOR

A. Suggested supplemental audiovisual

1. Flip-flops (E-89-363). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

MODULE: DIGITAL LOGIC APPLICATION

UNIT V: FLIP-FLOPS

LESSON 1: FLIP-FLOPS AND REGISTERS

I. Terms and definitions

A. Buffer--circuit that offers increased input impedance and extra gain

B. Complementary--opposite

C. Latch--storage element for a single bit of data

D. Prohibitive--condition that exists when Q and $\overline{Q}$ outputs on a flip-flop are not complementary

II. RS flip-flops

A. Flip-flops as storage elements

1. A flip-flop is a bi-stable device (two stable states).

2. A flip-flop is basically a storage element that can store one bit of data.

3. Most flip-flops have two outputs--the normal output and the complement of the output. However, in some cases, the normal output is the only one available.

4. When flip-flops are combined together to store multi-bit words, the circuit is called a register.

B. Low-active RS flip-flops (latch)

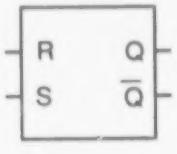
1. The RS flip-flop can be made two ways.

a. Cross-coupled NAND gates

b. Cross-coupled NOR gates

c. Cross-coupling is a method in which the output of one gate is fed back to the input of the other.

2. Schematic diagram symbol of an RS flip-flop



3. Truth table for an RS flip-flop breadboarded from cross-coupled NAND gates

R	S	Q	$\overline{Q}$	State
0	0	1	1	Prohibitive
0	1	0	1	Reset
1	0	1	0	Set
1	1	X	$\overline{X}$	Depends on previous state

RSFF (NAND)

4. Set flip-flop--storing a binary 1 in the Q output
Reset flip-flop--storing a 0 in the Q output

5. To determine the output of an RS flip-flop breadboarded from NAND gates, see which input, if any, receives a low.

   a. The input that receives the low determines what the output state will be.

      Example: If R receives a low and S receives a high, output Q will store a binary 0 (reset). If R receives a high and S receives a low, the Q output will store a binary 1 (set).

   b. If no input receives a low, the flip-flop will continue to store the previously stored number.

   c. If both inputs receive a low, the flip-flop will be prohibitive (also called ambiguous). (Both outputs will go to a binary 1. This condition is usually avoided.)

6. This flip-flop is called low active because whichever input receives the low determines the state of the flip-flop.

   NOTE: An I.C. with a bar over it is low active.

7. Unless both inputs are active (both inputs low), the outputs will always be opposite or complementary.

C. High-active RS flip-flop

1. Breadboarded from cross-coupled NOR gates

2. High active--input that receives the high determines what the flip-flop is storing

   a. If R receives a high and S receives a low, the flip-flop will store a binary 0 (reset).

   b. If R receives a low and S receives a high, the flip-flop stores a binary 1 (set).

   c. If no input receives a high, the flip-flop will continue to store the previously stored number.

   d. If both inputs receive a high, the flip-flop will be prohibitive (ambiguous). Both outputs go to a binary 0. This condition is usually avoided.

3. Truth table for a flip-flop breadboarded from cross-coupled NOR gates

R	S	Q	$\overline{Q}$	State
0	0	X	$\overline{X}$	Previous state
0	1	1	0	Set
1	0	0	1	Reset
1	1	0	0	Prohibitive

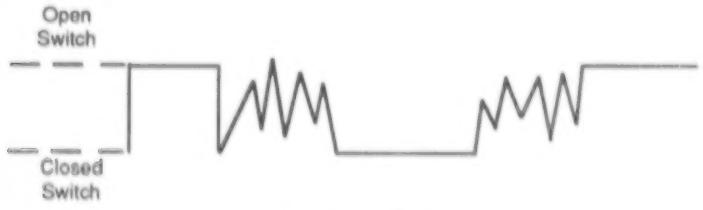
RSFF (NOR)

4. Unless both inputs are active (both inputs high), the outputs will always be opposite or complementary.
5. The schematic symbol is identical to that of the flip-flop breadboarded from cross-coupled NAND gates.

D. Applications for RS flip-flops

1. Use as switch debouncers (switch buffer latch)

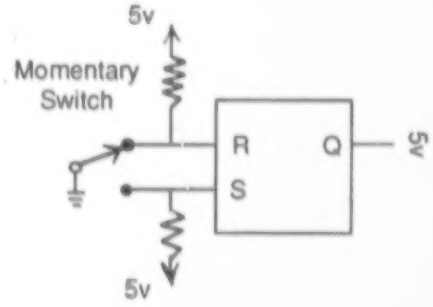
a. Push-button switches are used in digital circuits as input devices. When pressed these switches have a tendency to "bounce" because the contacts do not make a good electrical connection. This can appear as the waveform below.



Switch Bounce

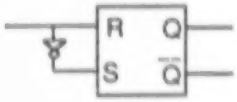
b. The bouncing of the switch can be regarded by the digital circuitry as a series of high-to-low transitions instead of just one.

c. RS flip-flops breadboarded from NAND or NOR gates can be used to latch the logic level input from the switch and pull up the resistor. Once the switch is closed and a low enters the R input, regardless of contact bounce, the flip-flop will go into a reset condition. When the button is released, the low enters the S input and the flip-flop returns to the set condition.



2. Use to store binary numbers

a. In the low-active RS flip-flop illustrated below, an invertor is placed between the R and S inputs; therefore, the inputs are always complementary.



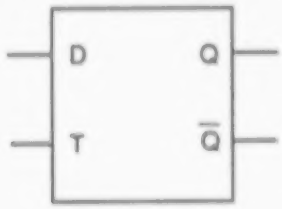
b. If a low enters the R input, the flip-flop stores a binary 0. If a binary 1 was present at the R input, S would go low. Therefore, the flip-flop would set, storing a binary 1.

III. D-type flip-flops (HO 1.1)

A. Construction and operation

1. Breadboarded from a combination of gates and an RS flip-flop; uses both NAND and NOR gates

2. Schematic symbol for a D-type flip-flop



3. Has two inputs and two outputs

a. The outputs are labeled Q and not $\overline{Q}$.

b. The outputs are always complementary.

c. Inputs are labeled D (data input) and T for time (sometimes referred to as CP--clock pulse). The latter is the control input.

4. Varieties of D-type flip-flops

a. High-active--stores whatever comes in on D only when T is high. If T is low, the flip-flop ignores D input and continues to store the previously stored input.

b. Low-active--stores whatever comes in on D only when T is low. If T is high, the flip-flop ignores D input and continues to store the previously stored input.

5. Truth tables for low-active and high-active D-type flip-flops

Low-active D-type

D	T	Q	$\overline{Q}$	State
0	0	0	1	Reset
0	1	X	$\overline{X}$	Previous state
1	0	1	0	Set
1	1	X	$\overline{X}$	Previous state

High-active D-type

D	T	Q	$\overline{Q}$	State
0	0	X	$\overline{X}$	Prev. state
0	1	0	1	Reset
1	0	X	$\overline{X}$	Prev. state
1	1	1	0	Set

6. Example: 7474 (dual D-type flip-flop). Examine the data sheet for this I.C. (HO 1.1, Illustration 1).

a. Pin 2 (D_1) is the D input of the first D-type flip-flop.

b. Pin 3 (CP_1) is the CP or T input of the first D-type flip-flop.

c. Pin 1 (R_{01}) is a low-active master reset that will reset the flip-flop no matter what the input is if a low is applied to it.

d. Pin 4 (S_D) is a low-active master set input that will set the flip-flop when a low is applied to it.

e. As with all digital I.C.s, one must connect the supply voltage and ground pins before the I.C. will work.

f. If both the master set and reset pins are taken low simultaneously, the Q and $\overline{Q}$ output will both go high. This is prohibitive or ambiguous.

g. The second internal D-type flip-flop is identical.

h. The 7474 can be used as an RS flip-flop by using the master reset and master set pins as the R and S inputs. In doing so, ignore the D and T inputs. This would create a low-active RS flip-flop. To create a high-active flip-flop, the inputs would have to be inverted.

B. Applications

1. D-type flip-flops are used mainly as storage devices for bits of data.

a. Can store a single bit of data (1 or 0) and the complement of the bit (The complement is usually not used.)

b. Registers for storing multi-bit binary words

2. Example: 74174--a Hex D-type flip-flop containing six D-type flip-flops. (HO 1.1, Illustration 2)

a. D0-D5 are the six data inputs. CP (toggle) represents all of the toggle line of the six D-type flip-flops connected together. There is no individual control of each flip-flop.

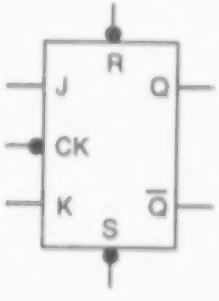
b. MR (master reset) is a control line. If a low is applied to MR, all outputs will reset.

c. A six-bit register (Registers are available in different sizes.)

IV. Construction and operation of JK flip-flops (HO 1.1)

A. Made from a combination of RS flip-flops and gates

B. Schematic diagram symbol



C. Has three inputs

1. J and K are the data inputs.

2. T or CK is for time--sometimes called CP (clock pulse). (Note that T may or may not have an inverted clock input.)

D. Edge-triggered flip-flop--will not set or reset unless a leading edge or trailing edge occurs, regardless of what is present on J or K. (Some varieties of JK flip-flops are leading-edge triggered, and some are trailing-edge triggered.)

E. There is a Q and $\overline{Q}$ output available (as with all flip-flops).

F. Truth table for a trailing-edge triggered JK flip-flop.

J	K	T	Q	$\overline{Q}$	State
0	0	↓	X	$\overline{X}$	Previous state
0	1	↓	0	1	Reset
1	0	↓	1	0	Set
1	1	↓	↕	↕	Toggles

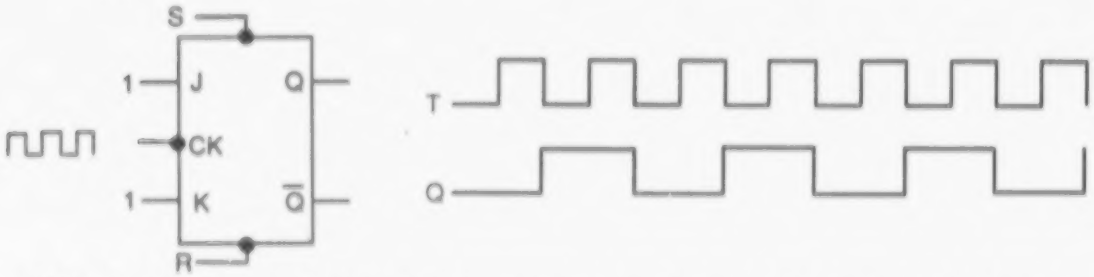
NOTE: The arrow pointing down means a high-to-low transition on this input.

G. Consider the J input as the set input and the K input as the reset input. The input with the high present will determine the output state of the flip-flop.

1. If J is high and K is low when a trailing edge occurs on T, the flip-flop will set.

2. If both J and K inputs are low when a trailing edge occurs on T, the flip-flop will continue to store the previous input.

3. If both J and K inputs are high, the flip-flop will change states on every trailing edge. The timing diagram below illustrates this point. Note that the output is half the frequency input T.



H. JK flip-flops have master set and master reset inputs that override J and K inputs to set and clear the flip-flop. The set and clear inputs do not require a leading or trailing edge input on T.

I. Truth table for the S (master set) and C (master reset) inputs of a JK flip-flop

S	C	Q	$\overline{Q}$	State
0	0	1	1	Prohibitive
0	1	1	0	Set
1	0	0	1	Reset
1	1	X	$\overline{X}$	Previous condition

1. These two inputs can be used to create a NAND (low active) RS flip-flop.

2. J, K and T inputs are not used. This eliminates the need for cross-coupling a NAND gate.

J. 7476--a popular JK flip-flop (There are many other varieties available.) (HO 1.1, Illustration 3)

V. Applications of flip-flops

A. Memory

1. I.C.s are used to store binary bits of information. (Memory is a vital part of a computer system.)

2. I.C.s with thousands of flip-flops inside are used for memory.

B. Counters

1. Flip-flops can be combined together to form binary counters.

2. Useful applications include incrementing through a program stored in a computer system's memory.

C. Registers

1. Groups of flip-flops used to store multi-bit binary words

2. Can temporarily store and manipulate data

TTL LOGIC DATA MANUAL EXCERPTS

Dual D-Type Flip-Flop

DESCRIPTION

The 'F74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F74	125MHz	11.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74F74N	
Plastic SO	N74F74D	
Ceramic DIP		S54F74F
Ceramic LLCC		S54F74G

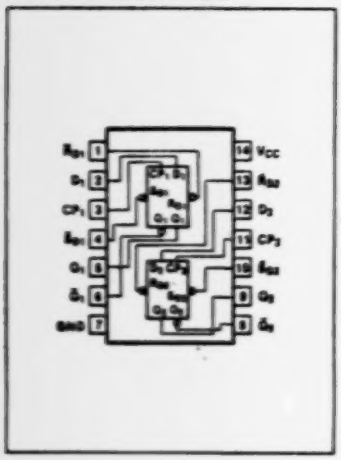
NOTE
SO package is surface-mounted micro-miniature DIP available 1984
LLCC is 20-pin surface-mounted leadless chip carrier

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

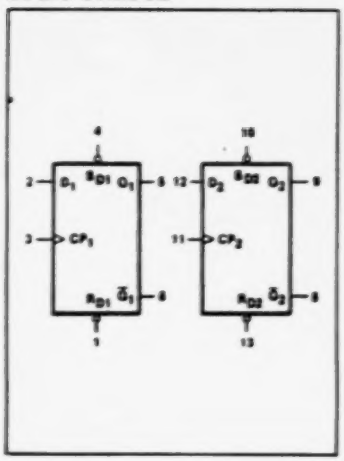
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_1, D_2	Data Inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset Inputs (Active LOW)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set Inputs (Active LOW)	1.0/3.0	20μA/1.8mA
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

Note
One (1.0) FAST unit load (U.L.) is defined as: 20μA in the HIGH state and 0.6mA in the LOW state

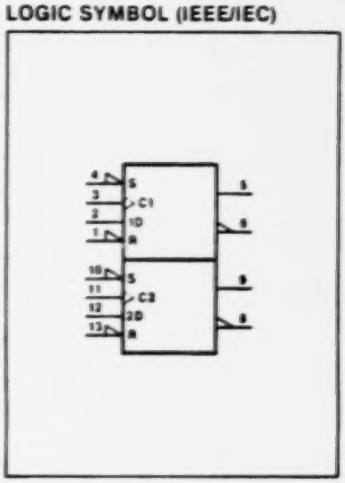
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Credit: TTL Logic Data Manual. Sunnyvale, Calif.: Signetics Company, 1982, pgs. 5-40, 5-125, 3-105.

Preview

Hex D Flip-Flop

- **Six edge-triggered D-type flip-flops**
- **Three speed-power ranges available**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74F174	100MHz	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = – 55°C to + 125°C
Plastic DIP	N74F174N	
Plastic SO	N74F174D	
Ceramic DIP		
Ceramic LLCC		

NOTE
SO package is surface-mounted micro-miniature DIP available 1984.
LLCC is 20-pin surface-mounted leadless chip carrier.

DESCRIPTION

The 'F174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

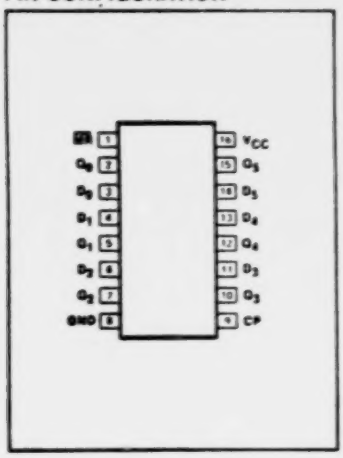
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and master Reset are common to all storage elements.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

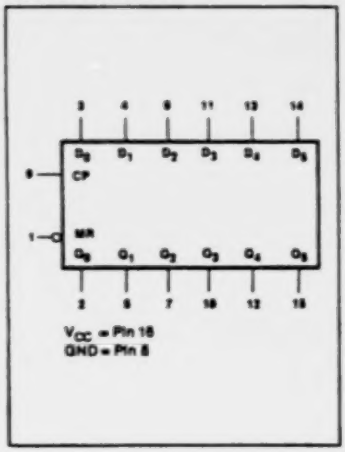
PINS	DESCRIPTION	54/74F (U.L.) High/Low	LOAD VALUE High/Low
D_0-D_5	Data Inputs	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input (Active Low)	1.0/1.0	20μA/0.6mA
Q_0-Q_5	Outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20μA in the HIGH state and 0.6mA in the LOW state.

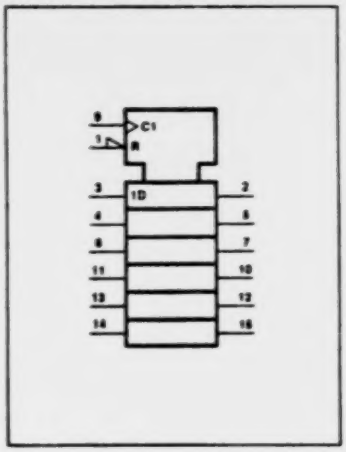
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual J-K Flip-Flop

DESCRIPTION

The '76 is a dual J-K flip-flop with individual J, K, Clock, Set and Reset inputs. The 7476 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW Clock transition.

The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the Clock and Data inputs, forcing the outputs to the steady state levels as shown in the Function Table.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7476	20MHz	10mA
74LS76	45MHz	4mA

ORDERING CODE

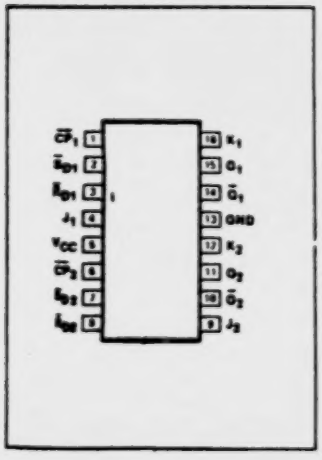
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7476N • N74LS76N	
Ceramic DIP	N7476F • N74LS76F	S5476F • S54LS76F
Flatpack		S5476W • S54LS76W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

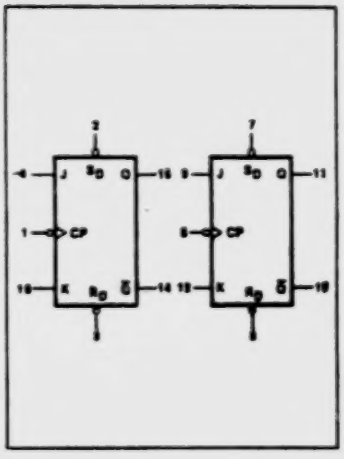
PINS	DESCRIPTION	54/74	54/74LS
$\overline{CP}$	Clock Input	2ul	2LSul
$\overline{R}_D$, $\overline{S}_D$	Reset and Set Inputs	2ul	2LSul
J, K	Data Inputs	1ul	1LSul
Q, $\overline{Q}$	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40µA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20µA I_{IH} and −0.4mA I_{IL}

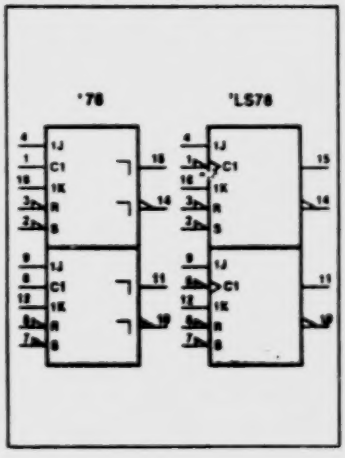
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

1. Name three types of flip-flops.

   a.

   b.

   c.

Define the following terms.

2. Latch--

3. Register--

4. Buffer--

5. Complementary--

6. Prohibitive--

7. Draw the schematic diagram symbols and truth tables for the three types of flip-flops.

8. Draw an RS flip-flop used as a switch debouncer.

9. Draw four JK flip-flops connected together to divide an input frequency of 1 KHz. What would the final output frequency be?

10. Which flip-flops do <u>not</u> become prohibitive?

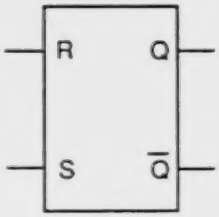
ANSWERS TO AS 1.1

1. RS, D-type and JK
2. Latch--storage element for a single bit of data
3. Register--flip-flops grouped together to store multi-bit binary words
4. Buffer--circuit that offers increased input impedance and extra gain
5. Complementary--opposite
6. Prohibitive--condition that exists when Q and $\overline{Q}$ outputs on a flip-flop are not complementary
7. Low active

R	S	Q	$\overline{Q}$
0	0	1	1
0	1	0	1
1	0	1	0
1	1	X	$\overline{X}$*

High active

R	S	Q	$\overline{Q}$
0	0	X	$\overline{X}$*
0	1	1	0
1	0	0	1
1	1	0	0



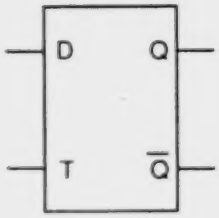
*Previous condition

Low active

D	T	Q	$\overline{Q}$
0	0	0	1
0	1	X	$\overline{X}$*
1	0	1	0
1	1	X	$\overline{X}$*

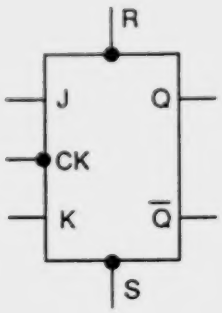
High active

D	T	Q	$\overline{Q}$
0	0	X	$\overline{X}$*
0	1	0	1
1	0	X	$\overline{X}$*
1	1	1	0

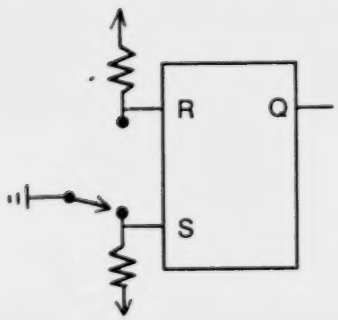


*Previous condition

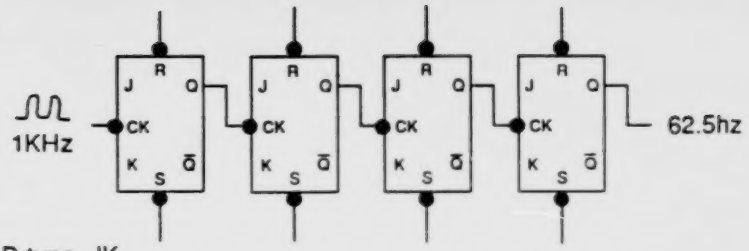
J	K	T	Q	$\overline{Q}$
0	0	↓	X	$\overline{X}$ Previous condition
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	X	$\overline{X}$ Changes state on every trailing edge



8.



9.



10. D-type, JK

USING AN RS FLIP-FLOP

Equipment:

1 - 7400
1 - 7402

Procedure:	Evaluation 3	2	1	N
1. Breadboard a NAND type RS flip-flop using a 7400.	—	—	—	—
2. Develop a truth table for the NAND RS flip-flop. Is this a high-active or low-active RS flip-flop?	—	—	—	—
3. Breadboard a NOR type RS flip-flop using a 7402.	—	—	—	—
4. Develop a truth table for the NOR RS flip-flop. Is this a high-active or low-active RS flip-flop?	—	—	—	—
Average of above evaluation*	—	—	—	—

*This average is the student's partial evaluation for competency K7: Construct combination logic circuits for a given application.

BREADBOARD A D-TYPE FLIP-FLOP

Equipment:

1 - 7474

Procedure:	Evaluation 3	2	1	N
1. Connect one of the D-type flip-flops inside the 7474.	—	—	—	—
2. Develop a truth table for the 7474. Is this a high-active or low-active D-type flip-flop?	—	—	—	—
3. Demonstrate proper operation of the flip-flop to the instructor.	—	—	—	—
4. Can the flip-flop's active state be reversed? If so, how?	—	—	—	—
5. Illustrate how two 7474 D-type flip-flops can be connected to form a four-bit register.	—	—	—	—
Average of above evaluation*	—	—	—	—

*This average is the student's partial evaluation for competency K7: Construct combination logic circuits for a given application.

BREADBOARD A JK FLIP-FLOP

Equipment:

1 - 7476
Oscilloscope

Procedure:	Evaluation 3	2	1	N
1. Connect one of the JK flip-flops inside the 7476.	—	—	—	—
2. Develop a truth table for the 7476. Remember, the flip-flop will not set or reset until a clock is applied. Develop a truth table for the 7476 using only the master set and reset inputs.	—	—	—	—
3. If you were to treat the master set and reset inputs as the R and S inputs of an RS flip-flop, would they have the same truth table? _____ Would this be a low-active or high-active device? (Circle your choice.)	—	—	—	—
4. Demonstrate proper operation of the flip-flop to the instructor.	—	—	—	—
5. Apply a clock pulse to the T input of the first JK flip-flop. Tie J and K high. The input frequency is _____ hertz.	—	—	—	—
6. Use an oscilloscope to monitor the Q output. The output frequency is _____ hertz. The output frequency is _____ the input frequency.	—	—	—	—
7. Tie the Q output of the first JK flip-flop to the T input of the second JK flip-flop inside the 7476. Tie the J and K inputs of the second JK flip-flop high. Monitor the output frequency. The frequency is _____ hertz. The output frequency of the second JK flip-flop is _____ the initial input frequency.	—	—	—	—
Average of above evaluation*	—	—	—	—

*This average is the student's partial evaluation for competency K7: Construct combination logic circuits for a given application.

CONSTRUCT FLIP-FLOPS AND DEVELOP TRUTH TABLES

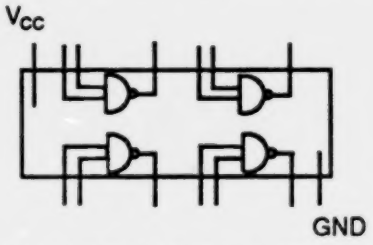
Equipment:

7400
7402
Oscilloscope

Procedure:

Evaluation 3 2 1 N

1. Breadboard a NAND-type RS flip-flop using a 7400. — — — —

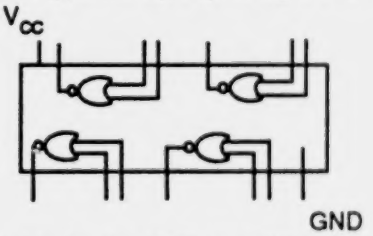


2. Develop a truth table for the NAND-type RS flip-flop. — — — —

R	S	Q	$\bar{Q}$	State
0	0			
0	1			
1	0			
1	1			

3. Verify the operation is correct by demonstrating it to the instructor. — — — —

4. Breadboard a NOR-type RS flip-flop using a 7402. — — — —



5. Develop a truth table for the NOR-type RS flip-flop. — — — —

R	S	Q	$\bar{Q}$	State
0	0			
0	1			
1	0			
1	1			

6. Verify the operation is complete by demonstrating it to the instructor. — — — —

Average of above evaluations* — — — —

*This average is the student's final evaluation for competencies K3 and K7.

MODULE: DIGITAL LOGIC APPLICATION

UNIT V: FLIP-FLOPS

UNIT TEST

Choose the option which best answers the question or completes the statement.

____ 1. How many stable states does a bi-stable device have?

a. One
b. Two
c. Four
d. Eight
e. None of the above

____ 2. What is a low-active RS flip-flop constructed from?

a. Cross-coupled NOR gates
b. Cross-coupled NAND gates
c. The master set and resets from a JK flip-flop
d. Both a and b
e. Both b and c

____ 3. Which of the following flip-flops can be used as a switch debouncer?

a. RS flip-flop
b. D type
c. JK flip-flop
d. Both a and c
e. All of the above

____ 4. Which type of flip-flop can be used as a frequency divider?

a. RS flip-flop
b. D type
c. JK flip-flop
d. Both a and c
e. Any of the above

____ 5. A NOR type RS flip-flop is set. The flip-flop receives a low at the R input. The flip-flop will _____.

a. Stay set
b. Reset
c. Go into a prohibitive state
d. Clear
e. None of the above

____ 6. A NOR type RS flip-flop is set. The flip flop receives a high at the R input. The flip-flop will _____.

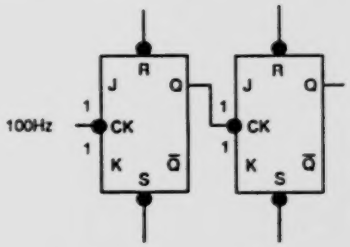
a. Stay set
b. Reset
c. Go into a prohibitive state
d. Clear
e. None of the above

___ 7. Most JK flip-flops are _____ devices.

a. Edge-triggered
b. High active
c. Low active
d. Non-transitional
e. Stationary

___ 8. What is the output frequency of the JK flip-flop below?

a. 1 KHz
b. 10 KHz
c. 20 KHz
d. 22 KHz
e. 25 KHz



___ 9. Which of the following is not an application of a flip-flop?

a. Memory
b. Counters
c. Registers
d. Decision-making
e. Storage

___ 10. When will a JK flip-flop reset?

a. K input is taken low and J input is taken high
b. K input is taken high and the J input is taken low
c. Master reset is taken low
d. Master set is taken high
e. Any of the above

___ 11. Which of the following describes a circuit that offers increased input impedance and extra gain?

a. Buffer
b. Complementary
c. Latch
d. Prohibitive
e. Transitional

___ 12. Which describes a condition that exists when Q and $\bar{Q}$ outputs on a flip-flop are not opposite?

a. Buffer
b. Complementary
c. Latch
d. Prohibitive
e. Transitional

ANSWERS TO UNIT TEST (K7)

1. b
2. b
3. a
4. c
5. a
6. b
7. a
8. e
9. d
10. c
11. a
12. d

MODULE: DIGITAL LOGIC APPLICATION

UNIT VI: COUNTERS AND SHIFT REGISTERS

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to construct counters and shift registers in SSI and MSI form, determine counter modulo, use counters as frequency dividers and construct circuits using shift registers. This knowledge will be evidenced by achieving the specified score on assignment sheets, job sheets and the unit test.

SPECIFIC OBJECTIVES

After completion of the lessons in this unit, the student should be able to:

1.1 Discuss classifications of counters. (competency K8)

1.2 Identify pure binary counter characteristics. (competency K8)

1.3 Construct programmable up/down circuits from JK flip-flops and logic gates. (competency K9)

1.4 Classify circuits as synchronous or asynchronous. (competency K8)

1.5 Discuss counter preset and reset capabilities. (competency K8)

1.6 Wire MSI pure binary and BCD counters. (competency K9)

1.7 Identify uses for special counters.

2.1 Explain the construction and operation of shift registers.

2.2 Identify types of shift registers.

2.3 Discuss shift register applications.

2.4 Wire a shift register, ring counter and Johnson counter. (competency K8)

MODULE: DIGITAL LOGIC APPLICATION

UNIT VI: COUNTERS AND SHIFT REGISTERS

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plans

1. Lesson 1: COUNTERS

   a. Information outline

   b. Handout

      HO 1.1: Counter data sheet

   c. Assignment sheet

      AS 1.1: Counters

   d. Answers to assignment sheet

   e. Job sheets

      JS 1.1: Wire JS flip-flops as up or down counters
      JS 1.2: Wire MSI pure binary and BCD counters

2. Lesson 2: SHIFT REGISTERS

   a. Information outline

   b. Handout

      HO 2.1 Shift register data sheet

   c. Assignment sheet

      AS 2.1: Shift registers

   d. Job sheet

      JS 2.1: Wire a shift register, ring counter and Johnson counter

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. Digital Techniques (Book 1 and 2). Benton Harbor, MI: Heath Co., 1986.

NOTES TO THE INSTRUCTOR

A. Suggested supplemental materials

1. TTL Logic Data Manual. Sunnyvale, CA: Signetics Company, 1982.

2. Registers and Counters (E-89-364). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

3. Counters and Dividers (E-89-365). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

MODULE: DIGITAL LOGIC APPLICATION

UNIT VI: COUNTERS AND SHIFT REGISTERS

LESSON 1: COUNTERS

I. Classifications

A. Digital counters are classified as sequential logic circuits.

B. Counters can also be classified as synchronous or asynchronous (ripple).

C. There are several different types of counters used in digital electronics.

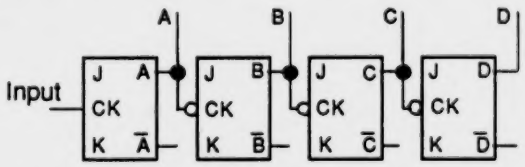
1. The pure binary counter counts only in binary.

2. The BCD counter counts in 8421 BCD format.

D. Counters can be constructed from JK flip-flops but are available in MSI integrated circuit form with many built-in features.

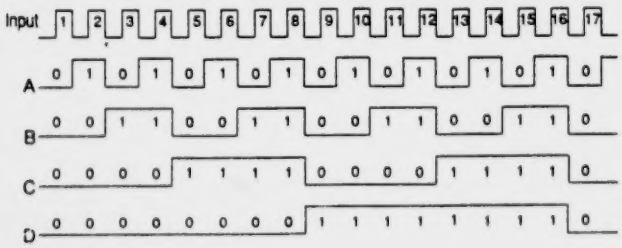
II. Pure binary counters (asynchronous)

A. A pure binary up counter can be constructed from cascaded JK flip-flops as shown below. In this configuration, each normal output is tied to the clock (CK) input of the next JK flip-flop.



B. Remember, a JK flip-flop will toggle or change states on every leading--or sometimes trailing--edge. This example will use a trailing-edge triggered (negative edge) flip-flop.

C. Examine the timing diagram and the count sequence for this circuit.



D	C	B	A	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	Recycle
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

D. It is important to note the count sequence and the frequency dividing action of the JK flip-flops as shown by the diagram.

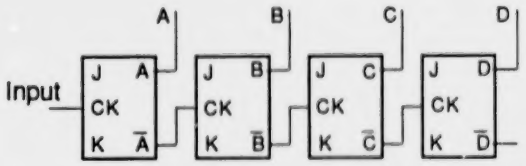
E. The output of a binary counter is always a sub-multiple of the power of two. Therefore, a counter can serve as a frequency divider as well as a counter.

F. The maximum count capability of a counter constructed from JK flip-flops can be calculated by using the formula $2^N - 1$, where N is the number of JK flip-flops.

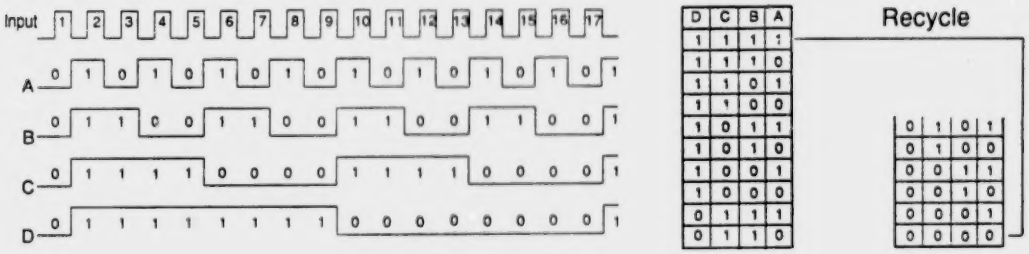
III. Up/down counters (asynchronous)

A. Down counters

1. A down counter can be formed by taking the outputs off the normal outputs as before, but driving the CK inputs from the previous complementary output instead.

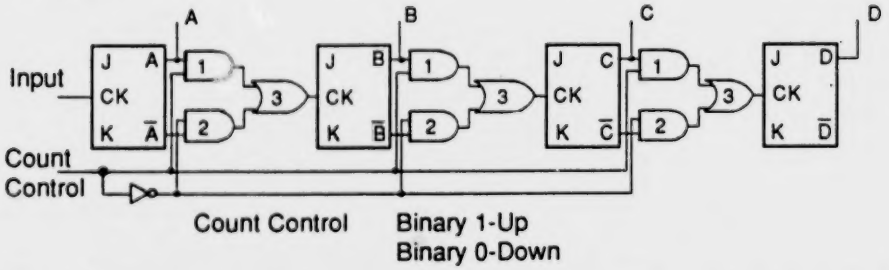


2. Note the count sequence and timing diagram for this circuit.



B. Programmable up/down counters

1. A programmable up/down counter can be constructed using external logic gates as shown below.



2. When count control input is high, all AND gates labeled "1" are enabled, allowing the CK input to be fed by the normal outputs. Thus, a count-up sequence is initiated.

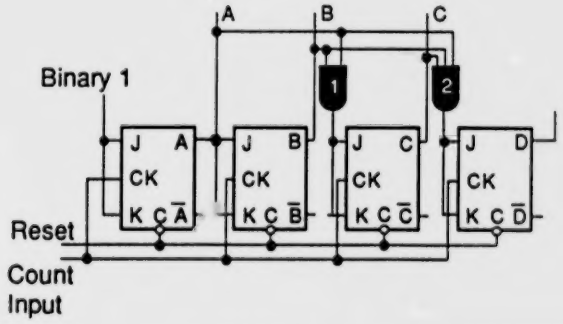
3. When count control input is low, all AND gates labeled "2" are enabled, allowing the CK input to be fed by the complementary outputs for a count-down sequence.

IV. Synchronous counters

A. Counters discussed thus far are classified as asynchronous or ripple counters because the input pulse must ripple through each flip-flop.

B. Ripple counters (asynchronous) are very straight-forward and easy to understand. However, the propagation delay of each flip-flop is additive, which will limit the high frequency range of the counter.

C. Synchronous counters are constructed from flip-flops that are all connected to a master clock at the same time, as shown below. They appear to be connected in parallel. (Asynchronous appear to be connected in series.)



D. Synchronous counters are capable of counting higher input frequencies since the clock pulse is applied to each flip-flop simultaneously. The propagation delay for the entire circuit is equal to that of a single JK flip-flop.

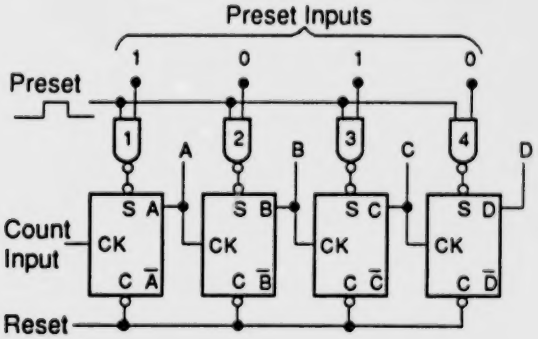
E. Examine the operation of the synchronous counter to verify its operation. AND gates 1 and 2 only allow the last two flip-flops to toggle when both inputs to the AND gates are high.

NOTE: Could this counter be made to count down? If so, how?

V. Preset and reset capability

A. Reset and preset of counters constructed from JK flip-flops is possible by using the master set and reset inputs of each JK.

B. To allow preset and reset capabilities, the circuit below is required.



1. When the preset control input goes high, NAND gates 1-4 are enabled, which allow the preset inputs to preset desired JK flip-flops.

2. Highs going into preset inputs come out of NAND gates low, presetting the JK. A low going into the NAND gate preset input exits a high and does not preset the flip-flop.

3. If preset control input is low, all NAND gates are disabled. No flip-flops will preset.

4. Since all the low active C (clear) inputs are tied together, a low on the reset input resets all flip-flops.

C. Other methods of preset and reset are possible, but all require some type of external logic.

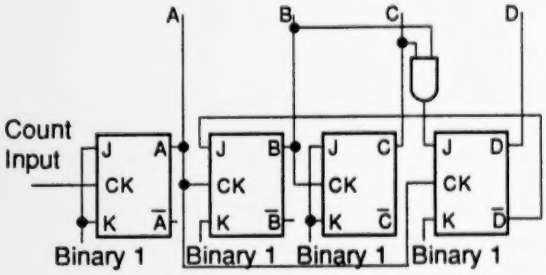
D. Programmability of up and down count, as well as preset and reset capability, can be done to create a counter with many features.

E. Counters can be purchased in MSI form that combine these features in an easy-to-use I.C. A typical MSI pure-binary counter is the 74193. (HO 1.1)

VI. BCD counters

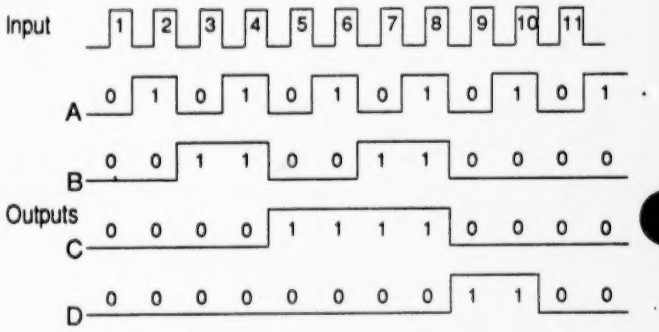
A. Pure binary counters count to the number calculated by the formula 2^N-1. BCD counters count to nine, then recycle to zero. BCD counters have 10 discrete states.

B. The count sequence, schematic diagram and timing diagram for an asynchronous BCD counter is illustrated below. Verify the operation of the BCD counter.



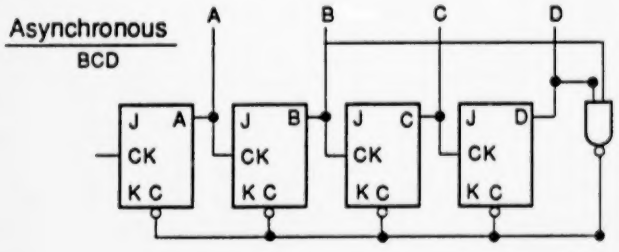
D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

Recycle



C. Notice the feedback path of the last complementary output to the J input of the second JK flip-flop. The two-input AND gate allows triggering of the last JK flip-flop only if the output of the second and third JK flip-flop are high.

D. A much easier method of creating a BCD counter is with the circuit shown below.

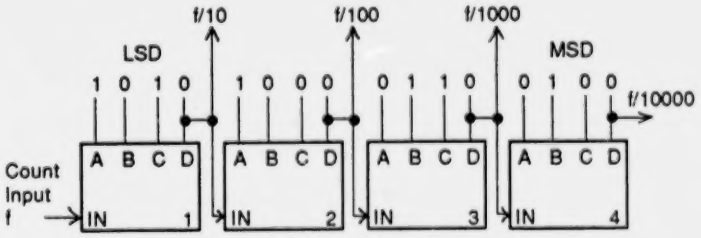


1. Normal outputs of the second and last JK flip-flop are NANDed together, and the output is applied to all of the low active clear inputs. Therefore, when the count sequence reaches 10, the counter clears (returns to zero).

2. The timing diagram and count sequence is identical that shown earlier.

3. This resetting method can also be used with a synchronous counter.

E. If a count sequence greater than 10 is needed, BCD counters can be cascaded to allow a count sequence as high as necessary. This is achieved by simply connecting the output of the MSB to the input of the next BCD counter, as shown below.



F. Since the output is in BCD, the number is easy to determine. The BCD output can now drive seven-segment decoder drivers in order to light up a seven-segment display.

G. BCD counters are available in MSI integrated circuits as illustrated with the 7490. (HO 1.2)

VII. Special counters

A. Gray counters

1. Capable of counting in Gray code

2. Very difficult to construct because of the count sequence

B. Counter modulo

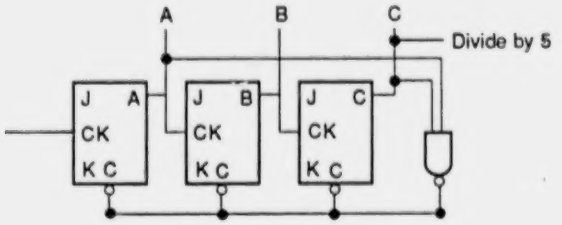
1. Modulo describes the number of discrete states or steps.

2. A BCD counter has a modulo of 10 since there are 10 discrete steps or states. It can be called a Mod 10 counter.

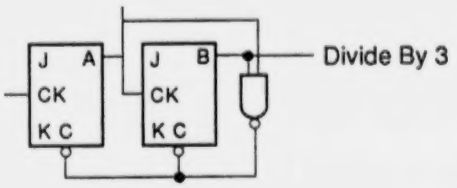
3. A pure binary counter made of four JK flip-flops is a Mod 16 counter because it has 2^4 discrete steps or states.

4. A counter of any modulo can be created by simply causing the counter to reset when the number of desired modulo is reached.

5. For example, a Mod 5 counter could be created by constructing the circuit below.



6. A modulo 3 counter is illustrated below.



C. Dividers

1. A counter can also be used as a divider.

2. If the output of a BCD counter is taken from the final JK flip-flop, the frequency is one-tenth the input. A BCD counter, therefore, could be used as a divide-by-10 divider.

3. Final output of a modulo 16 counter is one-sixteenth the frequency of the input (divide-by-16 divider).

4. The final output of a modulo 3 counter would be one-third the frequency of the input (divide-by-three divider).

5. Any multiple of division can be created simply by controlling the modulo of the count.

COUNTER DATA SHEET

JANUARY 1982

COUNTERS — 54/74192, 54/74193, LS192, LS19[illegible]

'192 Presettable BCD Decade Up/Down Counter
'193 Presettable 4-Bit Binary Up/Down Counter

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74192	32MHz	65mA
74LS192	32MHz	19mA
74193	32MHz	65mA
74LS193	32MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = – 55°C to + 125°C
Plastic DIP	N74192N • N74LS192N N74193N • N74LS193N	
Ceramic DIP	N74192F • N74LS192F N74193F • N74LS193F	S54LS192F S54193F • S54LS193F
Flatpack		S54LS192W S54193W • S54LS193W

DESCRIPTION

The '192 and '193 are 4-bit synchronous up/down counters — the '192 counts in BCD mode and the '193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either Clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up . . . if CP_D is pulsed while the CP_U is held HIGH, the device will count down. Only one Clock input can be held HIGH at any time; or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

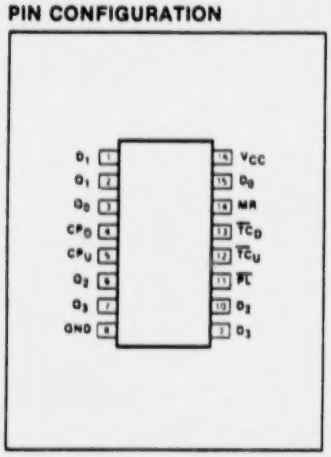
One clock should be held HIGH while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

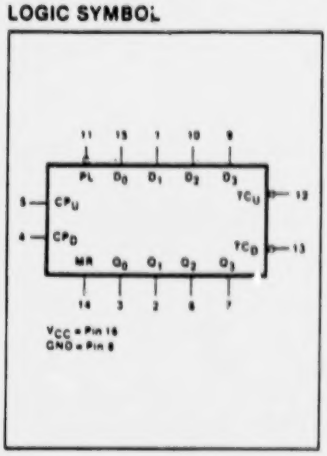
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40µA I_{IH} and – 1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20µA I_{IH} and – 0.4mA I_{IL}.

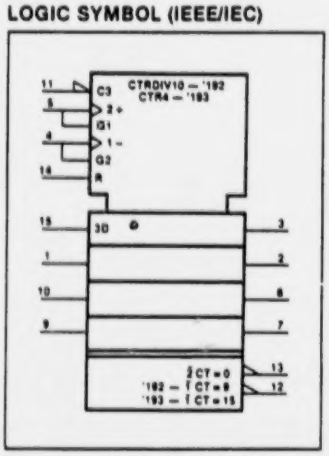
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Credit: TTL Logic Data Manual. Sunnyvale, CA: Signetics Company, 1982, pg. 3-339.

COUNTERS

Draw the following schematic diagrams.

1. Four-bit up counter using JK flip-flops

2. Four-bit down counter using JK flip-flops

3. Programmable four-bit up/down counter using JK flip-flops with master set and resets

4. Modulo 6 counter using JK flip-flops and external logic gates

Complete the following statements or questions.

____ 5. A modulo 6 counter is capable of frequency division by _____ .

a. .6
b. 6
c. 60
d. 600

____ 6. What is the maximum number a modulo 12 counter will count to?

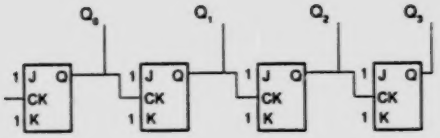
a. 6
b. 10
c. 11
d. 12

____ 7. A BCD counter has a frequency division of _____ .

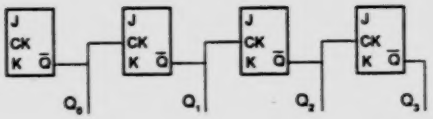
a. 2
b. 4
c. 8
d. 10

ANSWERS TO AS 1.1

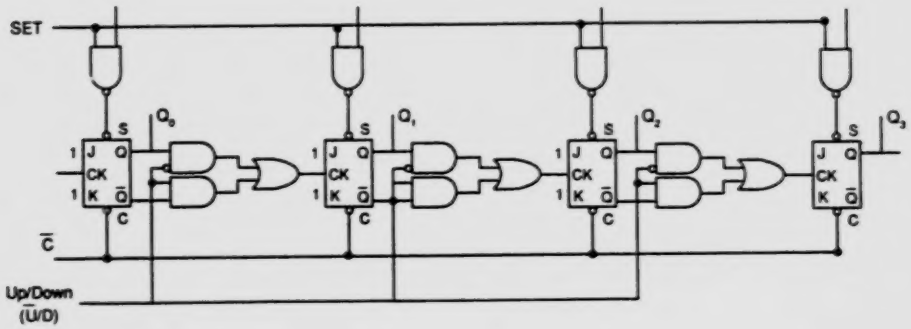
1.



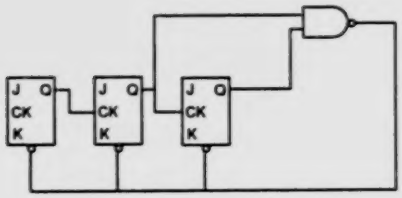
2.



3.



4.



5. b

6. c

7. d

WIRE JS FLIP-FLOPS AS UP OR DOWN COUNTERS

Equipment:

Two 7476 flip-flops

Procedure:	Evaluation 3	2	1	N
1. Draw the schematic diagram of a four-bit binary-up counter constructed from JK flip-flops.	—	—	—	—
2. Construct a four-bit binary-up counter from JK flip-flops.	—	—	—	—
3. Verify that the operation is correct; demonstrate the operation to the instructor.	—	—	—	—
4. Division of the initial input frequency is possible by 2, 4, 8 or 16. Explain where the output would be taken from to accomplish this for each divider.	—	—	—	—
a. 2				
b. 4				
c. 8				
d. 16				
5. Draw the schematic diagram of a four-bit binary-down counter constructed from JK flip-flops.	—	—	—	—
6. Construct a four-bit binary-down counter from JK flip-flops.	—	—	—	—
7. Verify that the operation is correct; demonstrate the operation to the instructor.	—	—	—	—
Average of above evaluations*	—	—	—	—

*This average is the student's partial evaluation for competency K9: Construct counter and controller circuits for sequential logic applications.

WIRE MSI PURE BINARY AND BCD COUNTERS

Equipment:

74192 counter
Two 74193 counters
7490 counter
Basic 7400 series logic gates, as needed

Procedure:	Evaluation 3	2	1	N
1. Draw the schematic diagram of the pin connections necessary to connect a **74192** as a simple up counter with reset capability.	—	—	—	—
2. Construct the circuit drawn above.	—	—	—	—
3. Verify that the operation is correct; demonstrate it to the instructor.	—	—	—	—
4. Division of the initial input frequency is possible by 2, 4, 8 or 16. Explain where the output would be taken from to accomplish this for each divider.	—	—	—	—
a. 2				
b. 4				
c. 8				
d. 16				
5. Draw the schematic diagram of the pin connections necessary to connect a 74192 as a simple down counter with reset capability.	—	—	—	—
6. Construct the circuit drawn above.	—	—	—	—
7. Verify the operation by demonstrating counter operation and reset capability to the instructor.	—	—	—	—

8. Draw the schematic diagram of the pin connections necessary to connect a **74193** as a simple up counter with reset capability. — — — —

9. Construct the circuit drawn above. — — — —

10. Verify that the operation is correct by demonstrating to the instructor. — — — —

11. Division of the initial input frequency is possible by 2, 4, 8 or 16. Explain where the output would be taken from to accomplish this for each divider. — — — —

    a. 2

    b. 4

    c. 8

    d. 16

12. Draw the schematic diagram of the pin connections necessary to connect a 74193 as a simple down counter with reset capability.

13. Construct the circuit drawn above. — — — —

14. Verify the operation by demonstrating counter operation and reset capability to the instructor.

15. Draw the schematic diagram of an eight-bit pure binary-up counter constructed from two 74193s with reset capability. — — — —

16. Construct the circuit drawn in the previous step. — — — —

17. Verify the operation by demonstrating counter operation and reset capability to the instructor. — — — —

18. Make the necessary changes to make the counter count down. — — — —

19. Verify the operation by demonstrating counter operation and reset capability to the instructor. — — — —

20. Draw the schematic diagram of the pin connections necessary to connect a **7490** as a simple up counter with set and reset capabilities. — — — —

21. Construct the circuit drawn above. — — — —

22. Verify the operation by demonstrating counter operation with set and reset capability to the instructor. — — — —

23. The 7490 connected with external logic gates can be used to create any desired counter modulo between one and nine. Draw the schematic diagram of the 7490 with external logic gates to create a modulo of five. — — — —

24. Construct the circuit drawn above. — — — —

25. Verify that the operation is correct by demonstrating the counter's operation to the instructor. — — — —

26. Determine frequency division of this circuit. ____ hz — — — —

Average of above evaluations* — — — —

*This average is the student's partial evaluation for competency K9: Construct counter and controller circuits for sequential logic applications.

MODULE: DIGITAL LOGIC APPLICATION

UNIT VI: COUNTERS AND SHIFT REGISTERS

LESSON 2: SHIFT REGISTERS

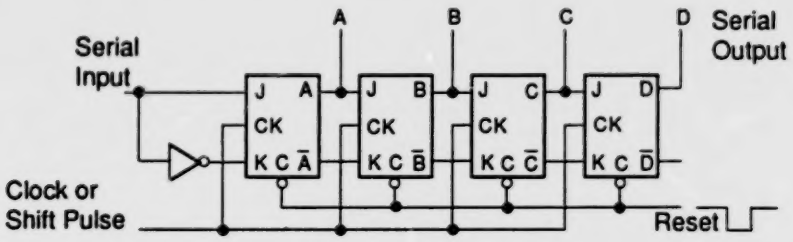
I. Basic construction and operation

A. A shift register is classified as a sequential logic circuit.

B. Shift registers do exactly what the name implies--shift bits from one flip-flop to the next to perform various logic functions.

C. Shift registers are usually constructed from flip-flops.

D. Construction of a shift register consisting of a JK flip-flop is illustrated below.



1. On a four-bit shift-right register, the J and K inputs of the first JK flip-flop are inverted. This ensures the J and K inputs will be complementary. If serial input is high, then J is high and K is low.

   a. On a trailing edge of CK, the first JK flip-flop will set. If serial input is low, then J is low and K is high.

   b. On a trailing edge of CK, the first JK flip-flop will reset. From then on, the stored bit shifts to the right through the register--hence the name, four-bit shift-right register.

   c. The register can be cleared by applying a low to the clear input.

2. This circuit is synchronous in operation since the clock is applied to all CK inputs simultaneously.

E. The 7495 (HO 1.2) is an MSI shift register which can perform shift left, shift right, serial load-serial output, serial load-parallel output, parallel load-serial output, parallel load-parallel output.

II. Types of shift registers

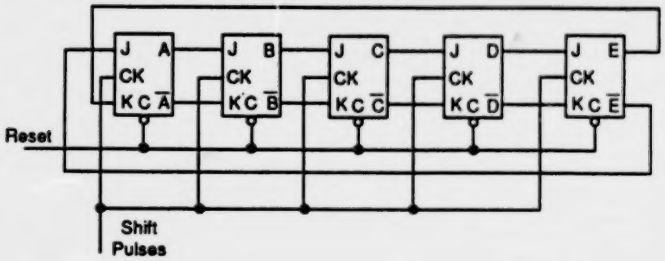
A. Shift registers are available in bipolar or MOS form.

B. Because of the high-density characteristics of MOS, shift registers that can store 256 eight-bit words are available. These registers actually store 2048 bits of data which can be manipulated.

C. MOS shift registers come in two varieties--dynamic and static.

1. Dynamic shift registers require a clock pulse to retain memory.

2. Static shift registers do not need a clock pulse to retain memory.



STATE	A	B	C	D	E
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Recycle

III. Applications of shift registers

A. Shift registers are capable of serial-to-parallel conversion when connected in serial load-parallel output configuration.

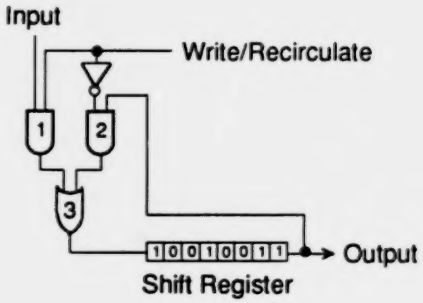
B. Shift registers are capable of parallel-to-serial conversion when connected in parallel load-serial output configuration.

C. Shift registers can multiply or divide by the power of two.

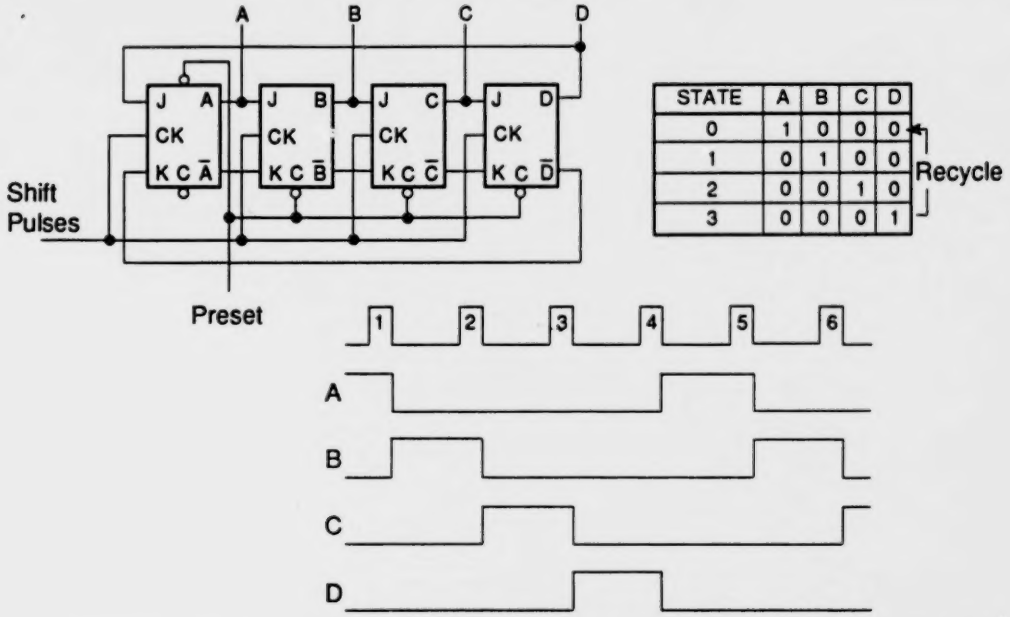
1. If the LSB is the left-most bit and data is shifted right, the number is divided by two.

2. If the number is shifted left, it is multiplied by powers of two. The opposite happens if the LSB is the right-most bit.

D. A shift register is capable of recirculating data stored in memory, as shown below. If the write/recirculate bit is a logic 1, a write operation will occur. If write/recirculate is a logic low, the data will recirculate with every clock pulse.



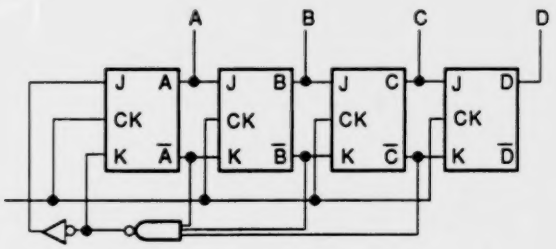
E. A ring counter or sequencer typical of the logic circuit necessary to perform the sequencing found on scanners is shown below. The counter or bit patterns is recirculated through the shift register since the output flip-flop is tied to the input flip-flop.



STATE	A	B	C	D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1

Recycle

F. A self-correcting ring counter or sequencer is illustrated below. On initial power-up, the flip-flops can start out in any state, set or reset. After the shift register completes one cycle, all flip-flops will be reset except for one.



G. With a Johnson Counter, shown under types of shift registers (Roman numeral II), only one stage changes state at each count.

1. Since the complement output of the last flip-flop is tied to the J input of the first JK flip-flop, the normal output is tied to the K input of the first JK flip-flop. This inverts bit patterns as they are recirculated through the register, which results in the count sequence shown above (self-correcting ring counter).

2. Although the output is not a weighted number system, it does produce 10 discrete states.

SHIFT REGISTERS 54/7495, LS95B

4-Bit Shift Register

- Separate negative-edge-triggered shift and parallel load clocks
- Common mode control input
- Shift right serial input
- Synchronous shift or load capabilities

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (Total)
7495	36MHz	36mA
74LS95B	36MHz	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7495N • N74LS95BN	
Ceramic DIP	N7495F • N74LS95BF	S5495F • S54LS95BF
Flatpack		S5495W • S54LS95BW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
S	Input	2ul	1LSul
Other	Inputs	1ul	1LSul
Q	Output	10ul	10LSul

NOTE

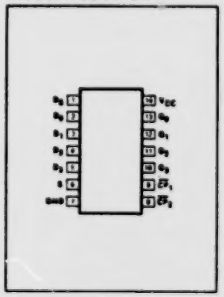
DESCRIPTION

The '95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has serial Data (D_S) and four parallel Data (D_0–D_3) inputs and four Parallel outputs (Q_0–Q_3). The serial or parallel mode of operation is controlled by a Mode Select input (S) and two Clock inputs ($\overline{CP}_1$ and $\overline{CP}_2$). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected Clock input.

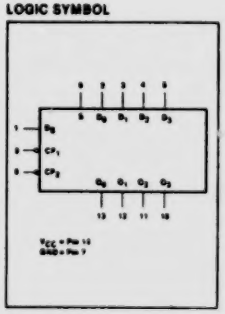
When the Mode Select input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_2$ loads parallel data from the D_0–D_3 inputs into the register. When S is LOW, CP_1 is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_1$ shifts the data from Serial input D_S to Q_0 and transfers the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (shift right). Shift left is accomplished by externally connecting Q_3 to D_2, Q_2 to D_1, Q_1 to D_0, and operating the '95 in the parallel mode (S = HIGH).

In normal operations the Mode Select (S) should change states only when both Clock inputs are LOW. However, changing S from HIGH-to-LOW while $\overline{CP}_2$ is LOW, or changing S from LOW-to-HIGH while $\overline{CP}_1$ is LOW will not cause any changes on the register outputs.

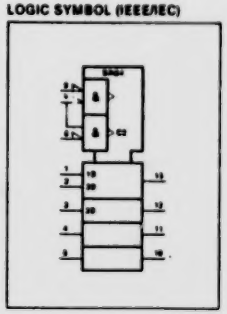
PIN CONFIGURATION



LOGIC SYMBOL

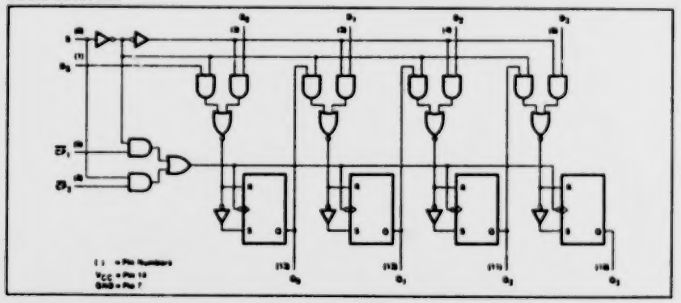


LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTERS 54/7495, LS95B

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{in} Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{in} Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A Operating free-air temperature range	−55 to +125		0 to 70		°C

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS S	CP_1	CP_2	D_S	D_n	OUTPUTS Q_0	Q_1	Q_2	Q_3
Parallel load	H	X	↓	X	l	L	L	L	L
	H	X	↓	X	h	H	H	H	H
Shift right	L	↓	l	X	X	L	q_0	q_1	q_2
	L	↓	h	X	X	H	q_0	q_1	q_2
Mode change	↑	L	X	X	X	no change undetermined			
	↑	H	↓	X	X	no change undetermined			
	↑	X	L	X	X				
	↑	X	H	X	X				

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74 Min	54/74 Nom	54/74 Max	54/74LS Min	54/74LS Nom	54/74LS Max	UNIT
V_{CC} Supply voltage		Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage			2.0			2.0			V
V_{IL} LOW-level input voltage		Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK} Input clamp current					−12			−18	mA
I_{OH} HIGH-level output current					−800			−400	µA
I_{OL} LOW-level output current		Mil			16			4	mA
		Com'l			16			8	mA
T_A Operating free-air temperature		Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

BEST COPY AVAILABLE

Credit: TTL Logic Data Manual. Sunnyvale, CA: Signetics Company, 1982, pg. 3-144, 3-145.

SHIFT REGISTERS

1. List three applications of a shift register.

   a.

   b.

   c.

2. Explain the difference between static and dynamic shift registers.

Use data sheets, such as those in the TTL Logic Data Manual, to describe the following MSI I.C.s.

3. 7490--

4. 74192--

5. 74193--

6. 74169--

7. 7495--

ANSWERS TO AS 1.1

1. Any three of the following:
   Conversion from serial to parallel or parallel to serial
   Multiplication or division by the power of two
   Recirculating data stored in memory
   Sequencing operations found on scanners
   Resets flip-flop after one cycle
   Use in Johnson counters to shift one stage at a time

2. Dynamic shift registers require a clock pulse to retain memory, whereas static shift registers do not.

3-7. Evaluated to satisfaction of instructor (K11)

WIRE A SHIFT REGISTER, RING COUNTER AND JOHNSON COUNTER

Equipment:

Two 7476 flip-flops
7495 MSI shift register
One 7404 logic gate

Procedure:		Evaluation 3	2	1	N
1.	Draw the schematic diagram of a four-bit shift register constructed from JK flip-flops.	—	—	—	—
2.	Construct the circuit drawn above.	—	—	—	—
3.	Verify that the operation is correct by demonstrating the counter's operation to the instructor.	—	—	—	—
4.	Draw the schematic diagram of a ring counter constructed from a 7495 MSI shift register.	—	—	—	—
5.	Construct the circuit drawn above.	—	—	—	—
6.	Verify that the operation is correct by demonstrating the counter's operation to the instructor.	—	—	—	—
7.	Create a self-correcting ring counter by adding the necessary logic gates.	—	—	—	—
8.	Verify that the operation is correct; demonstrate the counter's operation to the instructor.	—	—	—	—
9.	Draw the schematic diagram of the a four-bit Johnson counter constructed from a 7495.	—	—	—	—
10.	Construct the circuit drawn above.	—	—	—	—

11. Verify that the operation is correct by demonstrating the counter's operation to the instructor. — — — —

Average of above evaluations* — — — —

*This average is the student's final evaluation for competency K9: Construct counter and controller circuits for sequential logic applications.

MODULE: DIGITAL LOGIC APPLICATION

UNIT VI: COUNTERS AND SHIFT REGISTERS

UNIT TEST

Choose the option which best completes the statement or answers the question.

___ 1. Digital counters are classified as what kind of circuits?

a. Combinational
b. Sequential
c. Decision-making
d. All of the above
e. None of the above

___ 2. What is another name for an asynchronous counter?

a. Sequential
b. Trickle
c. Ripple
d. Synchronous
e. Non-sequential

___ 3. A four-bit BCD counter will count from 0 to _____ , then recycle.

a. 4
b. 9
c. 10
d. 15
e. 18

___ 4. A four-bit pure-binary counter will count from 0 to _____ , then recycle.

a. 4
b. 9
c. 10
d. 15
e. 18

___ 5. In which counter classification are all flip-flops are tied to a master clock?

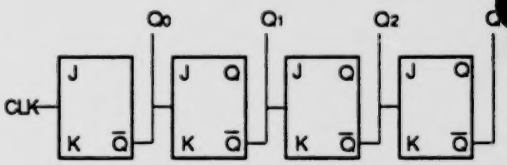
a. Sequential
b. Combinational
c. Synchronous
d. Asynchronous
e. None of the above

___ 6. When does the output of a JK flip-flop change states on every trailing edge CK?

a. J is high and K is low
b. J is low and K is high
c. Both J and K are low
d. Both J and K are high
e. Any of the above

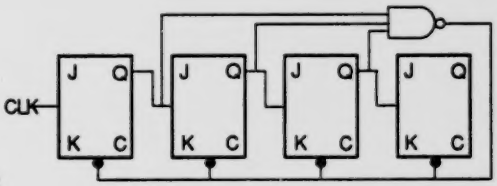
___ 7. In the binary counter illustrated below, what will the counter do on the next clock pulse?

a. Decrease
b. Increase
c. Stay the same
d. Reset
e. None of the above



___ 8. What is the modulo of the counter illustrated below?

a. Mod 6
b. Mod 7
c. Mod 8
d. Mod 9
e. Mod 10



___ 9. What does a 10-bit counter count to before recycling?

a. 10
b. 512
c. 820
d. 1023
e. 1024

___ 10. A Mod 15 counter counts to _____ and divides the input frequency by _____ .

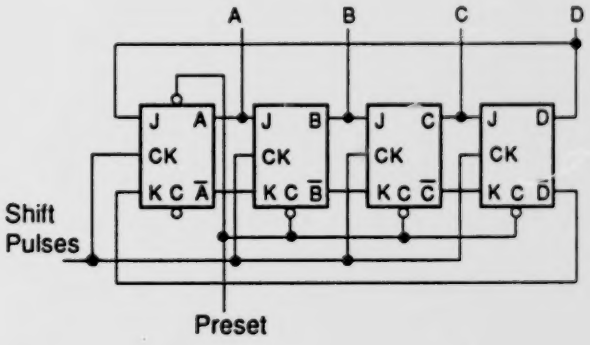
a. 14, 14
b. 14, 15
c. 15, 16
d. 15, 15
e. 16, 16

___ 11. Which one of the following is <u>not</u> an application of shift registers?

a. Counters
b. Memory
c. Logic
d. Scaling
e. Serial-to-parallel conversion

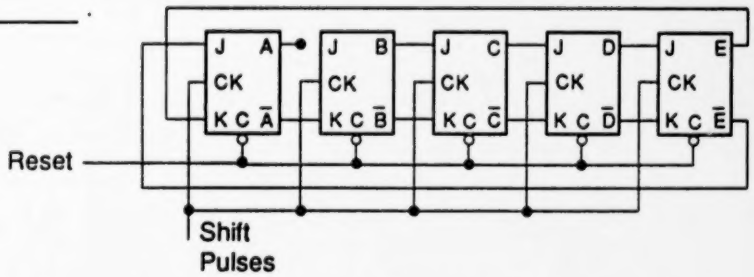
___ 12. What is the circuit below called?

a. Recirculating memory
b. A ring counter
c. A Johnson counter
d. A Gray counter
e. None of the above



___ 13. The circuit below is called _____ .

a. Recirculating memory
b. A ring counter
c. A Johnson counter
d. A Gray counter
e. None of the above



___ 14. The maximum count capability of a counter constructed from JK flip-flops can be calculated by using the formula _____ , where N is the number of JK flip-flops.

a. $2^N + 2$
b. $3^N - 1$
c. $2^N - 1$
d. $2^N + 1$
e. $2^N + 1$

___ 15. Which is needed for flip-flop preset and reset capability?

a. Some type of external logic
b. Use of the master set and reset inputs of each JK
c. NAND gates
d. All of the above
e. None of the above

___ 16. Shift registers are classified as _____ circuits.

a. Combinational
b. Sequential
c. Decision-making
d. All of the above
e. None of the above

___ 17. A shift register can perform _____ .

a. Shifts left
b. Shifts right
c. Serial load to serial output
d. Serial load to parallel output
e. All of the above

___ 18. Which is <u>not</u> a type of shift register?

a. Bipolar
b. MOS
c. Dynamic
d. BCD
e. JK

ANSWERS TO UNIT TEST (K8)

1. b
2. c
3. b
4. d
5. c
6. d
7. a
8. b
9. d
10. b
11. c
12. b
13. c
14. c
15. d
16. b
17. e
18. d

MODULE: DIGITAL LOGIC APPLICATION
UNIT VII: ENCODERS AND DECODERS

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to describe the operation of decoders and encoders. The student will also be able to construct and test decoder and encoder circuits. This knowledge will be evidenced by achieving the specified score on job sheets and the unit test.

SPECIFIC OBJECTIVES

After completion of the lessons in this unit, the student should be able to:

1.1 Analyze encoder operation.

1.2 Breadboard and test an encoder circuit. (competencies H6, K4)

2.1 Analyze decoder operation.

2.2 Analyze seven-segment operation.

2.3 Breadboard and test a decoder circuit. (competencies H6, K4)

MODULE: DIGITAL LOGIC APPLICATION

UNIT VII: ENCODERS AND DECODERS

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plans

1. Lesson 1: ENCODERS

   a. Information outline

   b. Assignment sheet

      AS 1.1: Analyzing encoder operation

   c. Answers to assignment sheet

   d. Job sheet

      JS 1.1: Breadboard and test an encoder circuit

2. Lesson 2: DECODERS

   a. Information outline

   b. Assignment sheets

      AS 2.1: Analyzing decoder operation
      AS 2.2: Analyzing seven-segment decoder operation

   c. Answers to assignment sheets

   d. Job sheet

      JS 2.1: Breadboard and test a decoder circuit

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. Forbes, Mark, and Barry B. Brey. Digital Electronics. Indianapolis, IN: Bobbs-Merrill Educational Publishing, 1984.

2. Hajek, Stanley M. Introduction to Digital Electronics. Albany, NY: Delmar, 1986.

3. Tocci, Ronald J. Digital Systems. 3rd ed. Englewood Cliffs, NJ: Prentice-Hall, 1985.

NOTES TO THE INSTRUCTOR

A. Suggested approaches to teaching this unit

1. For this unit, administer the unit test after job sheets are performed.

B. Suggested supplemental audiovisual

1. Encoders and Decoders (E-89-366). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

MODULE: DIGITAL LOGIC APPLICATION

UNIT VII: ENCODERS AND DECODERS

LESSON 1: ENCODERS

I. Encoders

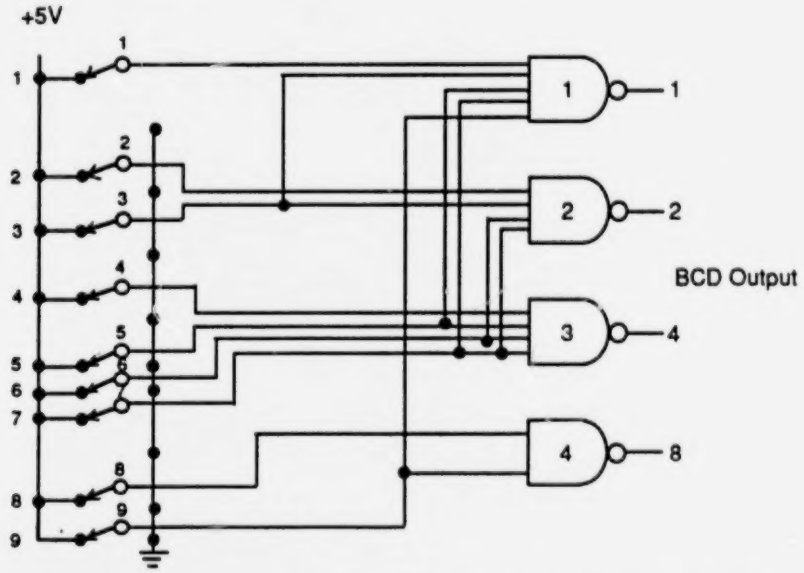
A. Encoders perform the opposite function of decoders.

B. Encoders are used to generate a coded output such as BCD or binary from a numeric input such as decimal.

Example: A digital calculator. The keyboard has decimal numbers and symbols. When a key is pressed, internal logic gates identify the number or symbol which has been pressed and converts it to binary for the calculator circuits.

C. Encoders are usually made up of AND, NAND, OR or NOR gates.

D. Shown below is a typical encoder circuit made up of NAND gates.



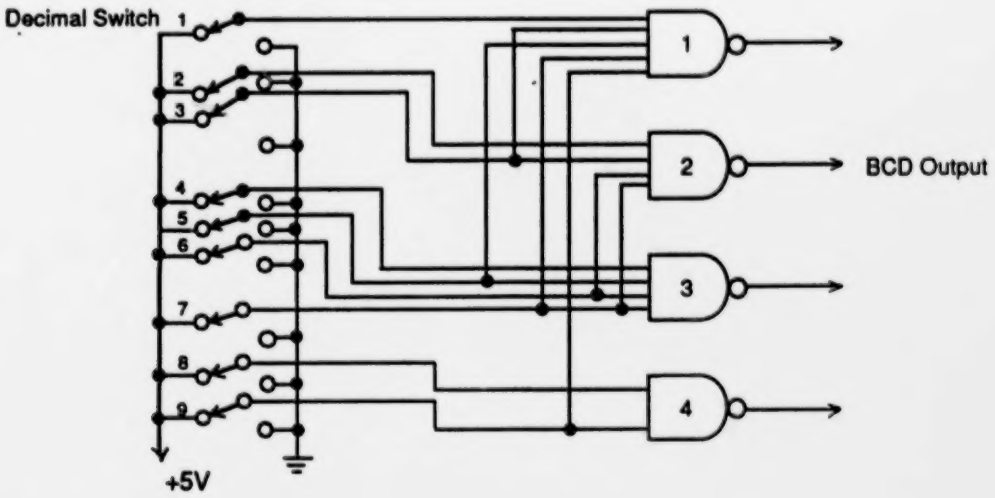
1. The NAND gate **inputs** represent decimal numbers 0-9, whereas NAND gate **outputs** represent BCD numbers 0000-1111.

2. When all switches are connected to the +5 volt line, a high (1) is applied to all NAND gate inputs. This action results in all NAND gate outputs becoming low (0). Since all NAND gate outputs are low (0), the BCD output is a binary 0000. This represents a decimal input of 0.

3. If the decimal value of three were selected on the input, switch 3 would be placed to ground (low). The remaining switches would be connected to +5 volts (high).

ANALYZING ENCODER OPERATION

From the following logic diagram of an encoder, determine which gates will be activated when the decimal numbers 1-9 are applied to the inputs.



	Decimal switch	NAND gates activated (1 at output)
___ 1.	1	
___ 2.	2	
___ 3.	3	
___ 4.	4	
___ 5.	5	
___ 6.	6	
___ 7.	7	
___ 8.	8	
___ 9.	9	

ANSWERS TO AS 1.1

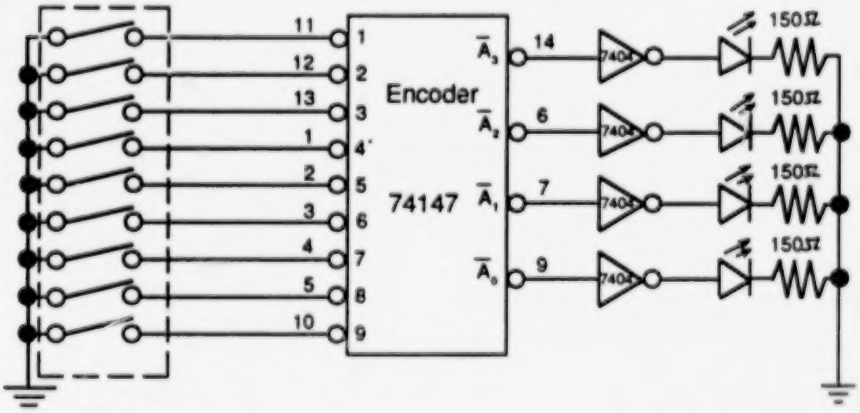
1. 1
2. 2
3. 1 and 2
4. 3
5. 1 and 3
6. 2 and 3
7. 1, 2 and 3
8. 4
9. 1, 4

BREADBOARD AND TEST AN ENCODER CIRCUIT

Equipment:

DIP switch, 10-position
7404 I.C.
74147 I.C.
Four 150Ω resistors
Five-volt DC power supply
Solderless breadboard

Procedure:	Evaluation 3	2	1	N
1. Insert the 74147 I.C., 7404 I.C. and 10-position DIP switch into the solderless breadboard.	—	—	—	—
2. Breadboard the circuit shown below.	—	—	—	—



3. Check circuit for correct wiring, then apply power. — — — —

4. Close switches 1-9 and record the BCD code displayed by the LEDs for each switch in the following table. — — — —

Input key Pressed	Outputs BCD code D	C	B	A
1				
2				
3				
4				
5				
6				
7				

Input key Pressed	Outputs BCD code D	C	B	A
8				
9				

5. Remove power and take down the circuit. Return parts to proper location. — — — —

Average of above evaluation* — — — —

*This average is the student's partial evaluation for competencies H6 and K4.

MODULE: DIGITAL LOGIC APPLICATION

UNIT VII: ENCODERS AND DECODERS

LESSON 2: DECODERS

I. Introduction

A. Decoding is the process of converting a code such as binary, BCD or hex into a more recognizable number or character.

B. The ability to translate codes is important in everyday life.

Examples: We can understand what we read because we know the English language code. In the supermarket, the bar codes on items selected are passed over a bar graph reader. The reader decodes this into a decimal display which indicates the price.

C. Decoders are very important in electronics.

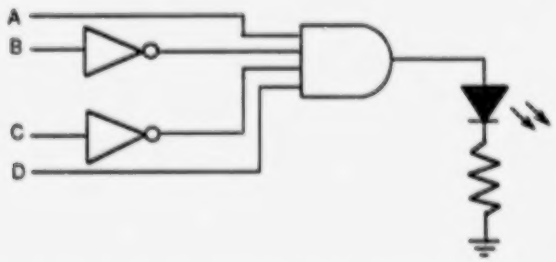
1. It is not difficult to understand different counting systems such as BCD and hex, but these systems can be awkward to use.

2. It would be inconvenient to enter a large number such as the decimal 9,180 in binary ones and zeros on a calculator. Also, most people would not want to decode a binary number such as 1100001010110.

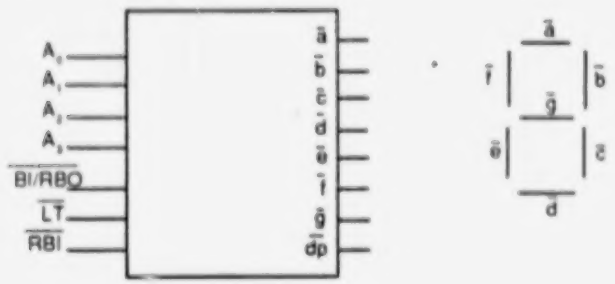
II. Seven-segment decoders

A. Decoders are made up of a combination of gates.

Example: A typical decoder for a binary nine. This decoder uses an AND gate and two inverters. The LED lights up only when the inputs are A = 1, B = 0, C = 0 and D = 1.



B. A popular decoder is the 7447 I.C. BCD-to-seven-segment decoder.



1. This decoder drives a seven-segment LED directly by accepting a four-bit BCD number and providing seven active-low, decoded outputs.

2. The 7447 is also used to drive multiplexed displays because it provides a 40mA output current capability.

3. The A0, A1, A2 and A3 inputs require highs for proper operation, while outputs a-g will be low to light a LED display.

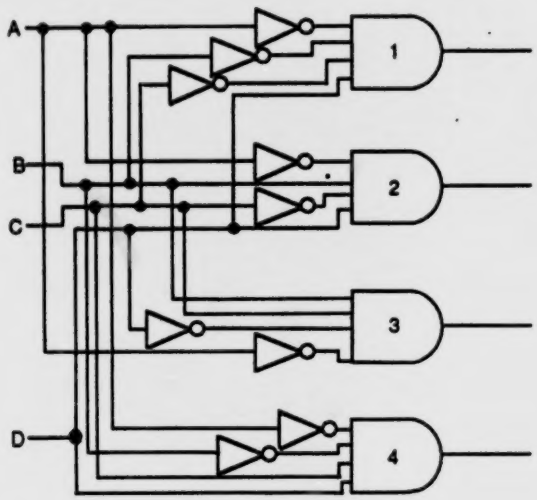
   Example: If the input A0 = 1, A1 = 1, A2 = 1 and A3 = 1 is applied, the output will be a = 0, b = 0, c = 0, d = 1, e = 1, f = 1 and g = 1. The decimal number seven will be displayed on the seven-segment display.

4. A convenient feature of the 7447 is that all seven segments can be tested for operation by applying a low to a pin labeled LT (LED test).

C. Other types of decoders are designed for other decoding functions and for different types of numbering systems.

ANALYZING DECODER OPERATION

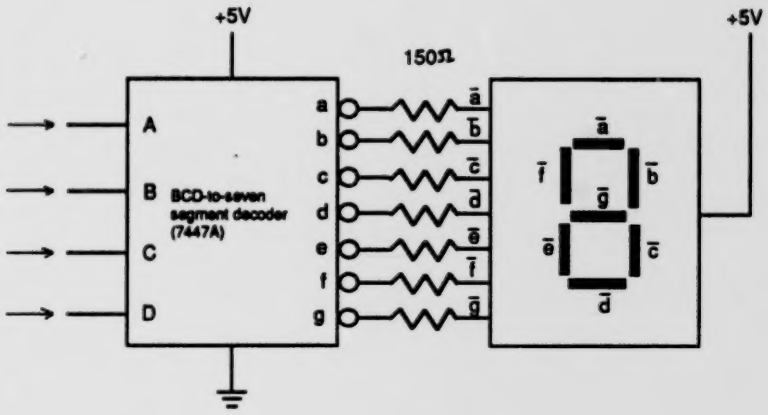
From the decoder logic diagram below, determine which AND gate will activate and the associated logic condition at its output for a given BCD input.



		BCD inputs D	C	B	A	Active AND gate	High/low logic condition
____	1.	0	1	1	0		
____	2.	1	0	1	0		
____	3.	1	0	0	0		
____	4.	1	1	0	0		

ANALYZING SEVEN-SEGMENT DECODER OPERATION

From the decoder logic diagram below, determine the logic conditions of the seven-segment outputs and the display for the given BCD inputs.



	BCD inputs D	C	B	A	Seven-segment outputs a	b	c	d	e	f	g	Display symbol
1.												
2.												
3.												
4.												
5.												
6.												
7.												
8.												
9.												
10.												

ANSWERS TO AS 2.1

1. 3, high
2. 2, high
3. 1, high
4. 4, high

ANSWERS TO AS 2.2

	BCD inputs				Seven-segment outputs							Display
	D	C	B	A	a	b	c	d	e	f	g	symbol
1.	0	0	0	0	L	L	L	L	L	L	H	0
2.	0	0	0	1	H	L	L	H	H	H	H	1
3.	0	0	1	0	L	L	H	L	L	H	L	2
4.	0	0	1	1	L	L	L	L	H	H	L	3
5.	0	1	0	0	H	L	H	L	H	L	L	4
6.	0	1	0	1	L	L	H	L	L	H	L	5
7.	0	1	1	0	H	H	L	L	L	L	L	6
8.	0	1	1	1	L	L	L	H	H	H	H	7
9.	1	0	0	0	L	L	L	L	L	L	L	8
10.	1	0	0	1	L	L	L	H	H	L	L	9

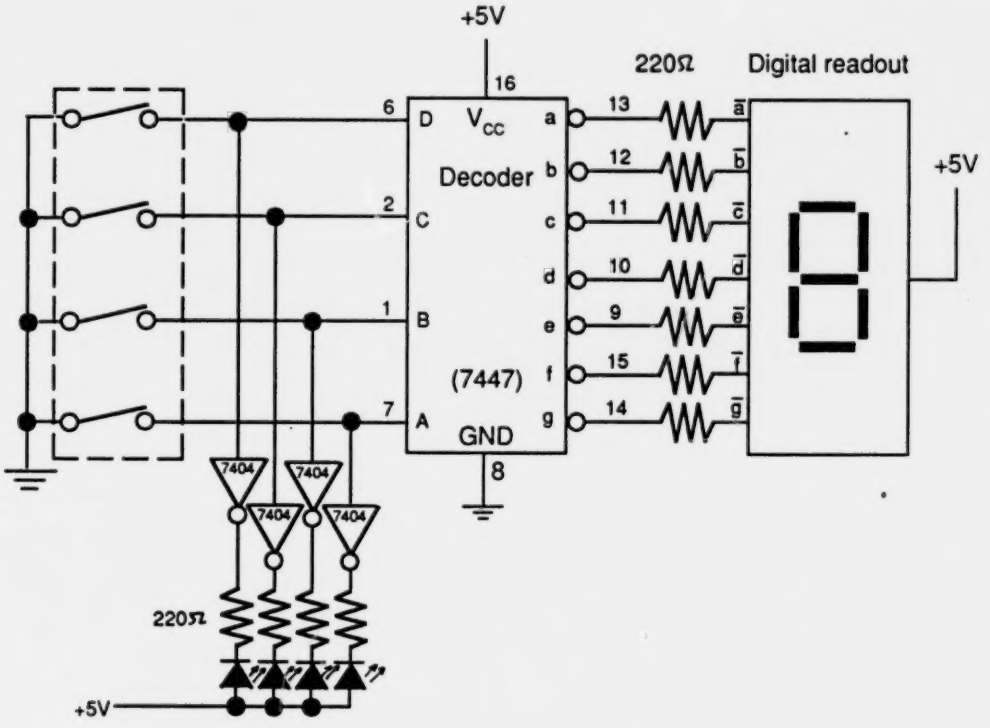
BREADBOARD AND TEST A DECODER CIRCUIT

Equipment:

7404 hex invertor I.C.
7447 BCD-to-seven-segment decoder I.C.
Seven-segment LED display (CA)
LED indicator lights (4)
220Ω, 1/4 watt resistor (11)
DC regulated power supply, 5V
Four-position DIP switch
Solderless breadboard

Procedure:

		Evaluation 3	2	1	N
1.	Insert the 7404 I.C., the 7447 I.C., the seven-segment display and four-position DIP switch into the solderless breadboard.	—	—	—	—
2.	Breadboard the circuit as shown below.	—	—	—	—



3.	Inspect wiring for shorts between resistors or wires.	—	—	—	—
4.	Apply power to the circuit.	—	—	—	—
5.	Turn all four DIP switches off (0000). The seven-segment display should display a zero decimal number.	—	—	—	—

6. Select each combination of BCD numbers 0000-1001 using the four-position DIP switches and record the results in the table below. — — — —

	BCD inputs				Seven-segment outputs							
	D	C	B	A	a	b	c	d	e	f	g	Display
a.	0	0	0	0								
b.	0	0	0	1								
c.	0	0	1	0								
d.	0	0	1	1								
e.	0	1	0	0								
f.	0	1	0	1								
g.	0	1	1	0								
h.	0	1	1	1								
i.	1	0	0	0								
j.	1	0	0	1								

7. Take down the circuit and return parts to their proper location. — — — —

Average of above evaluation* — — — —

*This average is the student's partial evaluation for competencies H6 and K4.

MODULE: DIGITAL LOGIC APPLICATION

UNIT VII: ENCODERS AND DECODERS

UNIT TEST

Select the option which best answers the question or completes the statement.

___ 1. What are encoders usually made up of?

a. Shift registers
b. Counters
c. Logic gates
d. Memory circuits
e. None of the above

___ 2. An encoder can be used to convert _____ .

a. From binary to decimal
b. From decimal to BCD
c. From BCD to seven-segment displays
d. Binary code to some other code
e. Any of the above

___ 3. An encoder with active high inputs means that _____ .

a. Only high inputs will activate the encoder outputs
b. Only LOW inputs will activate the encoder outputs
c. Either high or low inputs will activate the encoder outputs
d. The encoder outputs will always be low
e. None of the above

___ 4. How many inputs does a BCD-to-decimal decoder have?

a. Four
b. Eight
c. Ten
d. Sixteen
e. Twenty

___ 5. A decoder is required between a _____ .

a. Register and other circuits
b. Decimal keyboard and a latch circuit
c. Counter and BCD LED display
d. Decimal keyboard and seven-segment display
e. Counter and seven-segment display

___ 6. A BCD to seven-segment display decoder I.C. has an input that causes all outputs to become active. How is this input usually labeled?

a. RB/1
b. RB/2
c. LT
d. Strobe
e. RX

___ 7. A device is required that will convert BCD to decimal. What is this device normally called?

a. Decoder
b. Encoder
c. Multiplexer
d. Demultiplexer
e. None of the above

___ 8. Active-low outputs means that _____ .

a. 1s produce the desired action of a device
b. 0s produce the desired action of a device
c. All outputs are connected to a positive voltage
d. All outputs are connected to a negative voltage
e. None of the above

___ 9. What is required if a keyboard and a seven-segment display were used in a system, the system?

a. Only a decoder
b. Only an encoder
c. An encoder and decoder
d. An encoder and register
e. An encoder, decoder and register

___ 10. Four LEDs could be used to _____ .

a. Display a BCD code
b. Make a seven-segment display
c. Display the decimal numbers 0-9
d. Protect the input gate of an I.C.
e. None of the above

ANSWERS TO UNIT TEST (K4)

1. c
2. b
3. a
4. a
5. e
6. c
7. a
8. b
9. c
10. a

MODULE: DIGITAL LOGIC APPLICATION

UNIT VIII: ARITHMETIC CIRCUITS

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to add and subtract binary numbers. The student should be able to draw logic diagrams and construct and test for proper operation of full-adder, full-subtractor and four-bit adder/subtractor integrated circuits.

SPECIFIC OBJECTIVES

After completion of the lessons in this unit, the student should be able to:

1.1 Perform addition problems in binary according to general adder circuit rules.

1.2 Identify half-adder truth table, symbol and/or rules for addition.

1.3 Describe full-adder inputs and outputs.

1.4 Draw, wire and test a full-adder circuit. (competencies H6, K7)

2.1 Perform subtraction problems in binary according to general subtractor circuit rules.

2.2 Identify the half-subtractor circuit symbol, logic diagram and/or truth table.

2.3 Identify the full-subtractor circuit symbol, logic diagram and/or truth table.

2.4 Draw, wire and test a full-subtractor circuit. (competency K7)

3.1 Identify general information about adder/subtractor circuits.

3.2 Describe the operation of a four-bit full-adder/subtractor circuit.

3.3 Draw, wire and test a four-bit adder/subtractor circuit. (competency K7)

MODULE: DIGITAL LOGIC APPLICATION

UNIT VIII: ARITHMETIC CIRCUITS

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plans

1. Lesson 1: ADDER CIRCUITS

   a. Information outline

   b. Job sheet

      JS 1.1: Draw, wire and test a full-adder circuit

2. Lesson 2: SUBTRACTOR CIRCUITS

   a. Information outline

   b. Job sheet

      JS 2.1: Draw, wire and test a full-subtractor circuit

3. Lesson 3: ADDER/SUBTRACTOR CIRCUITS

   a. Information outline

   b. Job sheet

      JS 3.1: Draw, wire and test a four-bit adder/subtractor circuit

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. Kleitz, William. Digital Electronics, A Practical Approach. Englewood Cliffs, NJ: Prentice-Hall, 1987.

2. Tokheim, Roger L. Digital Electronics. 2nd ed. New York: McGraw-Hill, 1984.

NOTES TO THE INSTRUCTOR

A. Suggested approach to teaching this unit

1. The unit test can be used to prepare students for the job sheets and should be administered before job sheets are performed.

MODULE: DIGITAL LOGIC APPLICATION

UNIT VIII: ARITHMETIC CIRCUITS

LESSON 1: ADDER CIRCUITS

I. General information

A. Digital arithmetic is one of the most fundamental operations performed by a digital combination logic circuit. Arithmetic operations such as addition, subtraction, multiplication and division can be accomplished by a combination of gates and inverters.

B. The arithmetic operation performed by a digital circuit must use binary digits. There are four rules for binary addition.

A + B =	SUM	CARRY
0 + 0 =	0	0
0 + 1 =	1	0
1 + 0 =	1	0
1 + 1 =	0	1

C. As can be seen, the addition of two binary digits produces a two digit result, a SUM digit and a CARRY digit. When three digits are added in binary, the same rules apply. Following are the results.

A + B + C =	SUM	CARRY
0 + 0 + 0 =	0	0
0 + 0 + 1 =	1	0
0 + 1 + 0 =	1	0
0 + 1 + 1 =	0	1
1 + 0 + 0 =	1	0
1 + 0 + 1 =	0	1
1 + 1 + 0 =	0	1
1 + 1 + 1 =	1	1

D. As an example, add 7_{10} (base 10) and 6_{10} in binary.

		^{11} <---------Carry
7_{10}		0111
6_{10}	=	0110
13_{10}		1101

In the first column, 1 + 0 = 1. In the second column 1 + 1 = 0, carry 1. The carried digit is placed over the third column, which is 1 + 1 + 1 = 1, carry 1. The carried 1 is placed over the fourth column, which is 1 + 0 + 0 = 1.

E. Circuits that perform binary addition are constructed from basic gates (combination circuits) but are available as a single building block on an IC.

F. Binary addition differs from decimal addition in only one respect--when to carry.

1. The truth table for an exclusive OR gate will show that its results are identical to binary addition except for the carried digit, which results when both inputs are binary 1.

2. The circuit that performs addition, plus the carried digit, is called a **half-adder**.

TRUTH TABLE			
INPUTS		OUTPUT	
A	B	Y	
0	0	0	
0	1	1	
1	0	1	
1	1	0	<------CARRY 1

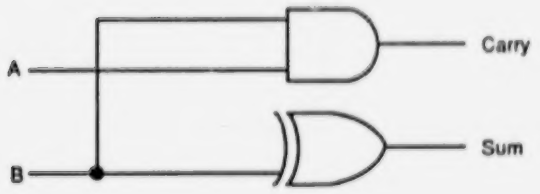
II. The half-adder

A. The circuit that performs addition, plus the carry, is called a half-adder.

1. As shown in the figure and table below, a half-adder is a logic circuit that can add two binary bits.

2. The circuit has two inputs, A and B, and two outputs, **sum** and **carry.** The carry function is the AND of the two inputs.

3. Inputs are A and B, and outputs are the **sum** (exclusive OR of A and B) and the **carry** (the AND of A and B).



Circuit for a half-adder

TRUTH TABLE			
INPUTS		OUTPUTS	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table for a half-adder

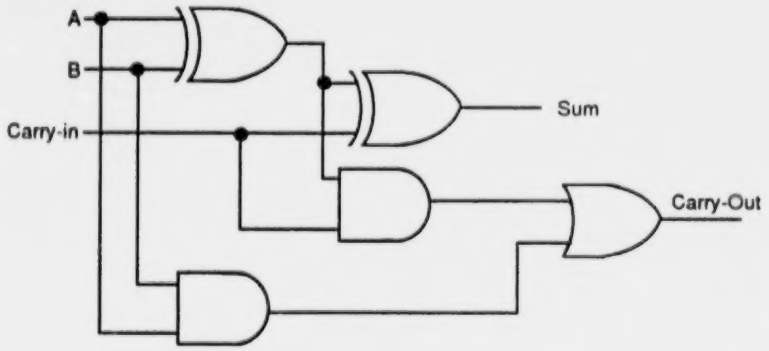
B. To simplify the diagram shown above, the symbol for a half-adder is usually represented by this symbol.

C. Although a half-adder can accept only two bits as inputs, any number of half-adders can be connected in parallel. If it is necessary to add three binary bits, two half-adders are used. The input of the second half-adder is the carry of the first half-adder, and the other input of the second half-adder becomes the input for the third bit.

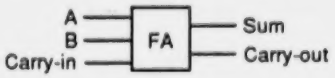
III. The full-adder

A. The full-adder accepts three inputs--two input bits and a carry input bit. These produce an output consisting of a sum and carry.

1. The carry input bit is normally referred to as the carry-in, and the carry output bit is normally referred to as the carry-out. The circuit is constructed by using two half-adders and an OR gate, as shown below.



2. The symbol for the full-adder is shown below.



B. The truth table for the full-adder is given below.

TRUTH TABLE

INPUTS			OUTPUTS	
A	B	CARRY-IN	SUM	CARRY-OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

DRAW, WIRE AND TEST A FULL-ADDER CIRCUIT

Equipment:

7408 AND gate I.C.
7432 OR gate I.C.
7486 XOR gate I.C.
Data sheets for integrated circuits
LED (2)
220Ω, 1/4 watt resistor (2)
Logic switches (3)
Solderless breadboard
22-gauge wire
5V DC power supply

NOTE: Use switches to simulate inputs and LEDs to indicate the result of the addition.

Procedure:	Evaluation 3	2	1	N
1. Draw a logic diagram of a full-adder circuit using gates indicated in the equipment list. Draw in switches for the inputs and LEDs with limiting resistors to indicate the output of the full-adder. Label all pin numbers.	—	—	—	—
2. Wire the full-adder circuit.	—	—	—	—
3. Apply power to the circuit. Ensure that correct voltages are applied to integrated circuits. Operate input switches and observe output indicator LEDs.	—	—	—	—
4. Apply inputs according to the chart below; enter output data in the space provided.	—	—	—	—

INPUTS			OUTPUTS	
C_{in}	B	A	Sum	Carry
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

5. Remove power, but leave the circuit wired for the next experiment. _ _ _ _

Average of above evaluations* _ _ _ _

*This average is the student's partial evaluation for competencies H6 and K7.

MODULE: DIGITAL LOGIC APPLICATION

UNIT VIII: ARITHMETIC CIRCUITS

LESSON 2: SUBTRACTOR CIRCUITS

I. General information

A. Combination logic circuits are used in making a subtractor circuit. Adders and subtractors are very similar. Use half-subtractors and full-subtractors in the same manner as half- and full-adders were used earlier.

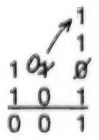
B. The rules for binary subtraction are as follows.

A - B =	Difference (Di)	Borrow (Bo)
0 - 0 =	0	0
0 - 1 =	1	1
1 - 0 =	1	0
1 - 1 =	0	0

C. The subtraction of two binary digits produces a two-digit result, a difference (Di) digit and a borrow (Bo) digit. Rules for binary subtraction will apply, regardless of the number of digits to be subtracted.

Example: $6_{10} - 5_{10}$ (in binary)

$6_{10} = 110_2$
$5_{10} = 101_2$
$1_{10} \quad 001_2$

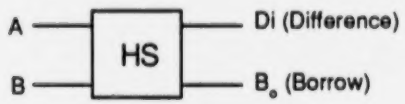


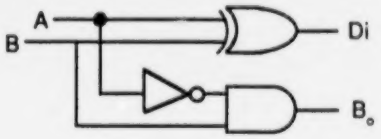
The computation on the left shows conversion from decimal to binary and the result of the subtraction. The computation on the right shows how a binary 10 is borrowed from the middle column to subtract the third column. The binary 10 from the middle column is equal to two binary 1's in the third column.

II. The half-subtractor

A. Inputs to a half-subtractor consists of the A input (minuend) and B input (subtrahend). Outputs consist of the A - B, difference (Di) output and the borrow (Bo) output.

B. The logic diagram and half-subtractor symbol are shown below.





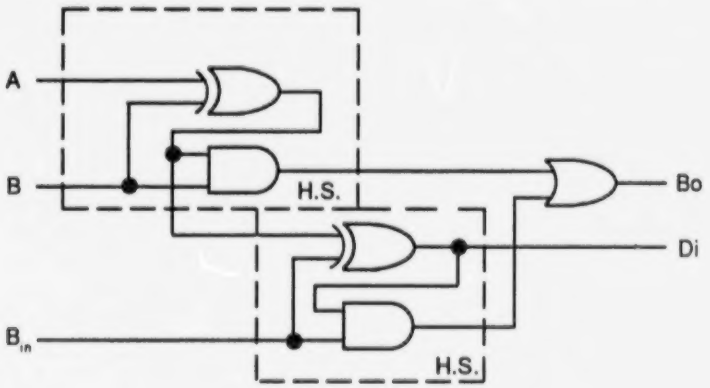
C. Truth table values applied to the circuit should prove the results of the truth table.

INPUTS		OUTPUTS	
A	B	Di	Bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

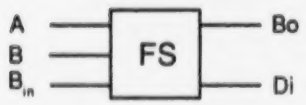
III. The full-subtractor

A. The full-subtractor allows a "borrow" from a previous subtractor to be input along with the subtrahend and minuend. The outputs are the difference and borrow-out.

B. The logic diagram is shown below. A full-subtractor is constructed from two half-subtractors, as is evident by the diagram.



C. The full-subtractor symbol and truth table are given below.



INPUTS			OUTPUTS	
A	B	B_{in}	Di	Bo
0	0	0	0	0
1	0	0	1	0
0	1	0	1	1
0	0	1	1	1
0	1	1	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

DRAW, WIRE AND TEST A FULL-SUBTRACTOR CIRCUIT

Equipment:

7404 hex inverter I.C.
7408 AND gate I.C.
7432 OR gate I.C.
7486 XOR gate I.C.
Data sheets for integrated circuits
LED (2)
220Ω, 1/4 watt resistor, (2)
Logic switches (3)
Power supply, DC
Solderless breadboard
22-gauge wire

NOTE: Use logic switches to simulate inputs and LEDs to indicate the result of the subtraction.

Procedure:		Evaluation 3	2	1	N
1.	Draw a logic diagram of a full-subtractor circuit using gates indicated in the equipment list. Draw in switches to control the input logic levels and LEDs to indicate the output of the full-subtractor. Label all pin numbers.	—	—	—	—
2.	Wire the full-subtractor circuit.	—	—	—	—
3.	Apply power to the circuit. Ensure that correct voltages are applied to the integrated circuits.	—	—	—	—

4. Operate the input switches according to the table below and observe output LEDs. Enter results in output column for each input. — — — —

INPUTS			OUTPUTS	
A	B	C	Di	Bo
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

5. Remove power. Take down the circuit and return parts to their proper place. — — — —

Average of above evaluations* — — — —

*This average is the student's partial evaluation for competency K7: Construct combination logic circuits for a given application.

MODULE: DIGITAL LOGIC APPLICATION

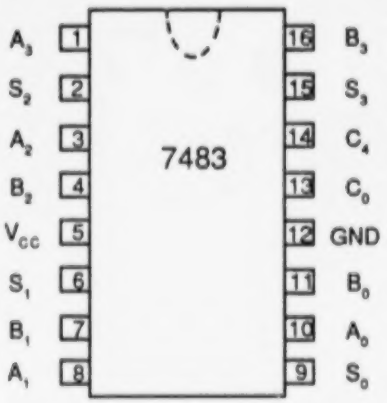
UNIT VIII: ARITHMETIC CIRCUITS

LESSON 3: ADDER/SUBTRACTOR CIRCUITS

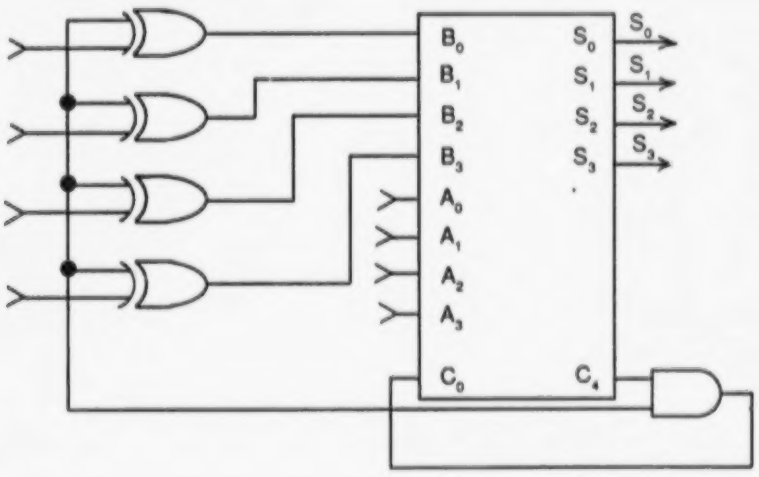
I. General information

A. The 7483 (TTL), 74HC283 (CMOS) and 4008 (CMOS) are medium-scale-integration (MSI) integrated circuits which contain four full-adders. They will add two four-bit binary words plus one incoming carry bit.

1. The 7483 pin diagram is shown to the right.



2. With the addition of four XOR gates and one AND gate, the 7483 can perform subtraction on two four-bit binary words. See diagram at right.



B. If a more advanced arithmetic circuit is required, the 74181 four-bit Arithmetic Logic Unit (ALU) can be used. This I.C. can perform the following functions.

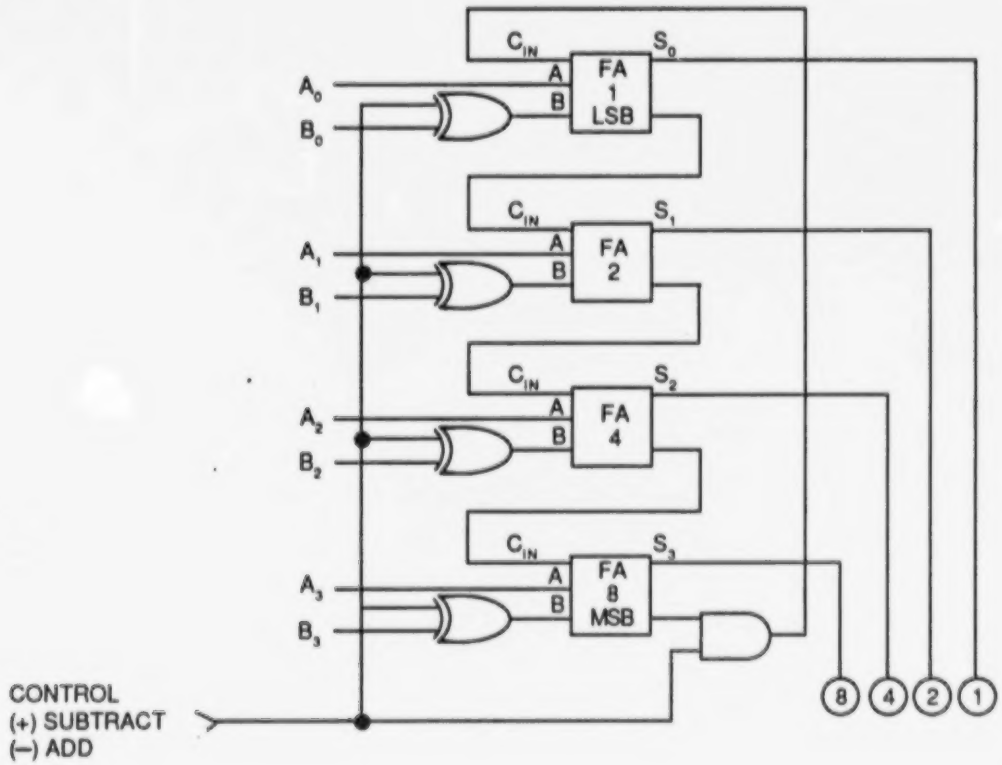
1. Provides 16 arithmetic operations: add, subtract, compare, double, plus 12 others

2. Provides 16 logic operations of two variables: exclusive-or, compare, AND, NAND, OR, NOR, plus 10 other logic operations

3. Full look ahead for high-speed arithmetic operation on long words

II. Four-bit full-adder/subtractor

A. A system can be designed that will add and subtract. See the illustration below.



B. A high input on the control line will set the system up for the subtraction mode of operation. A low input sets the system up for the addition mode.

C. When a low is placed on the control line, it is felt on the A inputs of the XOR gates and one input of the AND gate.

1. This low permits all bits on the B_0 through B_3 inputs to pass through the XOR gates non-inverted and applied to the inputs of the full-adders.

2. The full-adders add the two inputs, and the sum appears at the output indicators.

3. The low applied to the AND gate disables the AND gate during the addition mode of operation.

D. To change the circuit to a subtractor, a high is placed on the control line.

1. This causes a high to be placed on the XOR gates, which causes all bits on the B_0 through B_3 inputs to be inverted before they are applied to the full-adder.

2. This high is also placed on one input of the AND gate, which enables the AND gate.

3. The enabling of the AND gate will permit information from the MSB bit to be sent to the LSB full-adder.

4. The circuit subtracts B inputs from A inputs.

5. The difference (in binary form) appears at the output indicators.

DRAW, WIRE AND TEST A FOUR-BIT ADDER/SUBTRACTOR CIRCUIT

Equipment:

7404 hex inverter I.C.
7483 four-bit binary adder I.C.
I.C. data sheets
220Ω, 1/4 watt resistors (5)
LED (5)
Logic switches (8)
22-gauge wire
Solderless breadboard
Power supply, DC

NOTE: This exercise uses a 7483 four-bit binary adder I.C. to perform addition and subtraction of two four-bit digital words.

Procedure:	Evaluation 3	2	1	N
1. Draw the logic diagram for a four-bit binary adder using a 7483 I.C. Use eight logic switches to simulate two four-bit digital inputs. Use LEDs with limiting resistors to indicate the binary sum outputs. Remember to include an LED for the carry-out output. Label all pin numbers.	—	—	—	—
2. Wire the four-bit adder circuit.	—	—	—	—
3. Apply power to the circuit.	—	—	—	—

4. Add at least three different sets of numbers assigned by the instructor. Enter results below. — — — —

5. Remove power, but leave the circuit connected. — — — —

6. Draw the wiring diagram for a four-bit binary subtractor circuit using the 7483 I.C. Add inverters to each input of the B inputs. Connect the carry input and carry-out input together. Use eight logic switches for the four-bit inputs. Use LEDs with limiting resistors for the binary subtraction results. — — — —

7. Wire the four-bit subtractor circuit. Apply power to the circuit. — — — —

8. Subtract at least three sets of numbers assigned by the instructor. Enter results below. — — — —

9. Remove power. Take the circuit down and return parts to proper storage location. — — — —

Average of above evaluations* — — — —

*This average is the student's final evaluation for competency K7: Construct combination logic circuits for a given application.

MODULE: DIGITAL LOGIC APPLICATION

UNIT VIII: ARITHMETIC CIRCUITS

UNIT TEST

Select the option which best answers the question or completes the statement.

___ 1. What is the most significant bit of the binary number 10100?

a. 0
b. 1
c. 2
d. 10
e. Not determinable

___ 2. What is the sum of the binary numbers 1111 and 1010?

a. 1001
b. 1111
c. 1010
d. 10110
e. 11001

___ 3. What is the difference between the binary numbers 110011 and 1010?

a. 101001
b. 111001
c. 110011
d. 111011
e. 11010

___ 4. A full-adder circuit has how many inputs and outputs?

a. One
b. Two
c. Three
d. Four
e. Five

___ 5. To construct a four-bit parallel, what is needed?

a. Two full-adders and two XOR gates
b. Three full-adders and one half-adder
c. Four summing circuits
d. Four full-adders and four OR gates
e. Two full-adders and two OR gates

___ 6. To make a half-subiractor circuit from a half-adder, add a single _____ .

a. AND gate
b. OR gate
c. NOR gate
d. Inverter
e. XNOR gate

___ 7. Full-adder and full-subtractor circuits are classified as _____ .

a. Combination logic circuits
b. ECL circuits
c. MOS circuits
d. Sequential circuits
e. Registers

Refer to the 7483 I.C. data sheet to answer the following questions.

___ 8. The 7483 I.C. contains a four-bit binary _____ .

a. Register
b. Counter
c. Adder
d. Inverter
e. Subtractor

___ 9. The 7483 I.C. can be used to add _____ .

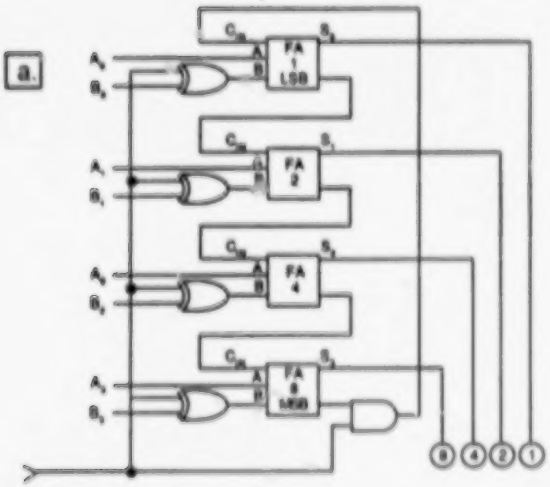
a. Two three-bit binary numbers
b. Two four-bit binary numbers
c. Three four-bit binary numbers
d. Either a or b
e. Any of the above

___ 10. To convert the 7483 I.C. to an adder/subtractor, four _____ gates and one _____ gate have to be added to the circuit.

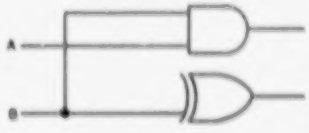
a. XOR, AND
b. NAND, XOR
c. XOR, INVERTER
d. AND, INVERTER
e. XNOR, AND

___ 11. Which of the following is the schematic diagram for a half-adder?

a.

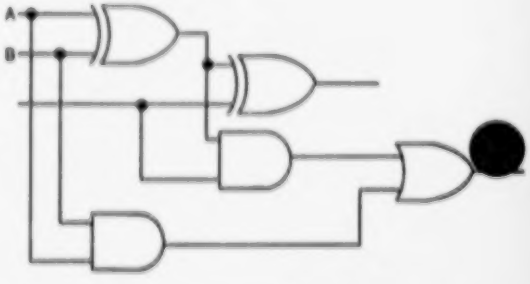


b.



c.

d.



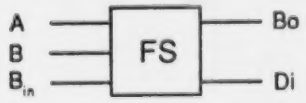
___ 12. Which of the previous drawings is the schematic for a half-subtractor?

___ 13. With a four-bit full-adder/subtractor circuit, a _____ on the control line will set the system up for the subtraction mode of operation. A _____ sets the system up for addition.

a. Low output, high input
b. Low input, high input
c. High input, low input
d. High input, low output
e. High input, high output

14. Draw the symbol for a full-subtractor circuit.

ANSWERS TO UNIT TEST

1. b (K7)
2. e (K7)
3. a (K7)
4. c (K7)
5. b (K7)
6. d (K7)
7. a (K7)
8. c (K11)
9. d (K11)
10. a (K11)
11. b (K7)
12. c (K7)
13. c (K7)
14. 

(K7)

MODULE: DIGITAL LOGIC APPLICATION

UNIT IX: MEMORY

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to breadboard a RAM circuit and identify differences between RAM, ROM, PROM and EPROM memory. This knowledge will be evidenced by achieving a specified score on the job sheet and unit test.

SPECIFIC OBJECTIVES

After completion of the lessons in this unit, the student should be able to:

1.1 Match terms and definitions related to random-access memory.

1.2 Describe characteristics of random-access memory (RAM).

1.3 Identify true statements about memory capacity.

1.4 Describe characteristics of the 7489 I.C.

1.5 Demonstrate the ability to breadboard and test a RAM circuit. (competencies K6 and K11)

2.1 Match terms and definitions related to read-only memory.

2.2 Describe characteristics of read-only memory (ROM). (competency K6)

2.3 Describe uses and make-up of a fuse link PROM.

2.4 Differentiate between EPROM, PROM, ROM and RAM memory.

MODULE: DIGITAL LOGIC APPLICATION

UNIT IX: MEMORY

CONTENTS OF THIS UNIT

A. Objective sheet

B. References

C. Notes to the instructor

D. Lesson plans

1. Lesson 1: RANDOM-ACCESS MEMORY

   a. Information outline

   b. Job sheet

      JS 1.1: Breadboard and test RAM

2. Lesson 2: READ ONLY MEMORY

   a. Information outline

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. TTL Data Book. Mountain View, CA: Fairchild Camera & Instrument Corp., 1978.

2. Hajek, Stanley M. Introduction to Digital Electronics. Albany, NY: Delmar, 1986.

3. Hoekstra, Robert L. Robotics and Automated Systems. Cincinnati, OH: South Western Publishing Co., 1986.

4. Kershaw, John D. Digital Electronics. 2nd ed. North Scituate, MA: Breton Publishers, 1983.

NOTES TO THE INSTRUCTOR

A. Suggested approaches to teaching this unit

1. In evaluating competency K6 (Describe the characteristics of ROMs and PLAs), please note that programmable logic arrays (PLAs) have not been discussed in this unit because RAMs and ROMs are more relevant to computers today.

B. Suggested supplemental materials

1. Manufacturer data sheets for 7404 and 7408 integrated circuits

2. Memory (E-89-367) (1/2" video). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

MODULE: DIGITAL LOGIC APPLICATION

UNIT IX: MEMORY

LESSON 1: RANDOM-ACCESS MEMORY

I. Terms and definitions

A. Address--common location in a memory occupied by a group of binary bits

B. Addressing--process of locating a specific location in a memory

C. Bit--binary digit

D. Byte--organization of binary cells or bits into small groups. In microprocessors, the byte is eight bits in length.

E. Enable--process of activating an integrated circuit

F. Nonvolatile--memory that is designed to retain its information even when its power is removed

G. RAM--random-access memory

H. Read--process of extracting data from a certain memory location

I. Register--memory word or area used for temporary storage of data

J. Write--process of loading information into memory

K. Volatile--memory that loses its information if power is removed

II. Random-access memory (RAM)

A. RAM is a group of registers that can be individually addressed, written into and read out of.

B. Most RAM circuits are in the form of integrated circuits made up of semiconductors. RAMs have been constructed with bipolar transistors, MOSFETs and magnetic cores.

C. Semiconductor memories can be either static or dynamic.

1. Static RAM

a. This type of RAM is volatile--data can be stored only as long as power is applied to the RAM. When power is removed, data is lost.

b. Bipolar or static flip-flops are used to store data.

c. Each flip-flop can store one bit of data. If the flip-flop is set, a binary 1 is stored. If the flip-flop is reset, a binary 0 is stored.

d. Several flip-flops are grouped to hold a binary word.

2. Dynamic RAM

   a. Contains capacitors and MOSFETs that store the data

   b. When the capacitor is discharged, a binary 0 is stored. When the capacitor is charged, a binary 1 is stored.

   c. Stored data must be refreshed every few milliseconds by a special clock circuit because capacitor charges leak off.

III. Memory capacity

A. Addressing uses a binary code to select a specific register location.

B. The "write" process places data into a specific register.

C. The "read" process retrieves data from a register location. Data stored in the register is not changed or destroyed.

D. The number of memory locations in which data can be stored, written into or read out from is commonly referred to as the number of registers.

1. K indicates the number of registers.

   a. A 1K (kilobyte) memory system has 1024 registers.

   b. A 64K memory system has 65,536 registers.

2. The number of bit storage areas in each register is also usually specified.

   a. A 16 x 4 (16 by 4) memory indicates that there are 16 registers which can each hold a four-bit word.

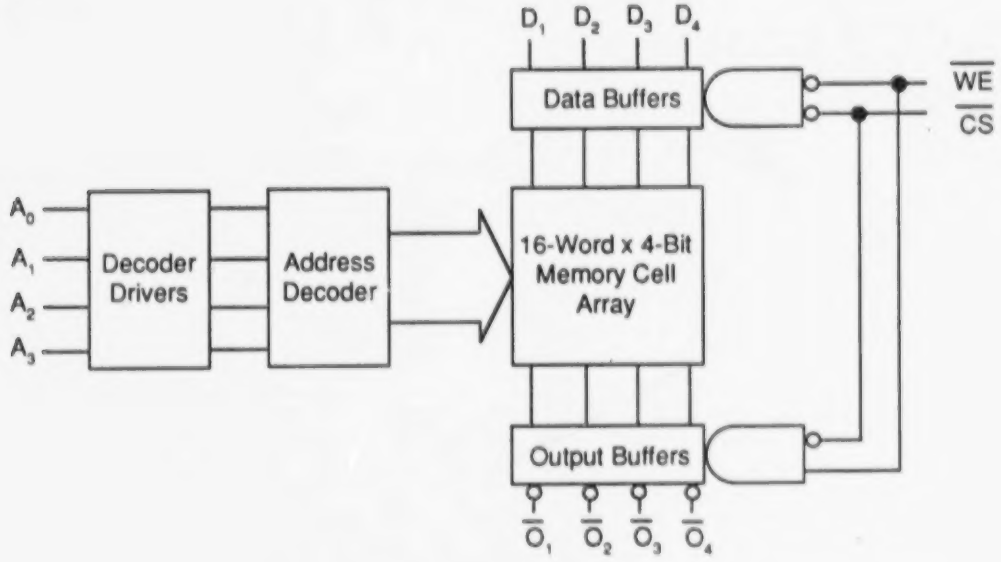
   b. If each register in a certain memory had eight flip-flops and 1024 registers, the memory would be referred to as a "1K by 8" memory.

IV. 7489 I.C. RAM operation

A. The 7489 is a 16 x 4 RAM circuit with limited memory. It is an excellent example for learning the basic operation of RAMs.

B. This I.C. is made up of 16 different registers, each capable of storing a four-bit data word. A total of 64 bits can be stored.

C. The logic diagram of the 7489 I.C. follows. RAM controls identified in the diagram are explained below.



1. The **chip select** ($\overline{CS}$) input is connected to ground (logic 0) to activate the I.C.
2. The **write enable** ($\overline{WE}$) input must be at a logic 0 when data is written into the RAM. $\overline{WE}$ must be at a logic 1 when data is read from the RAM.
3. **Address lines** (A0-A3) are used to select address 1-16.
4. **Data** inputs (D1-D4) are used to enter a four-bit data word into the selected address.
5. The **inverted data** outputs (Q1-Q4) provide the inverted binary-word output stored at a specific address when addressed.

D. Writing a word into a memory slot is done by applying the appropriate BCD number to the address lines, placing $\overline{CS}$ and $\overline{WE}$ at logic 0 and applying the bits stored at the data input lines D1-D4.

E. Reading a word is done by selecting the word's storage register by applying address bits to the address lines. If the first register is to be selected, a binary 0000 is applied to the address lines. If the second register is to be selected, a binary 0001 is applied. $\overline{CS}$ is placed at a logic 0 and $\overline{WE}$ is placed at logic 1. The complement of the word being addressed then appears at data outputs D1-D4.

F. The 7489 I.C. RAM has a volatile memory.

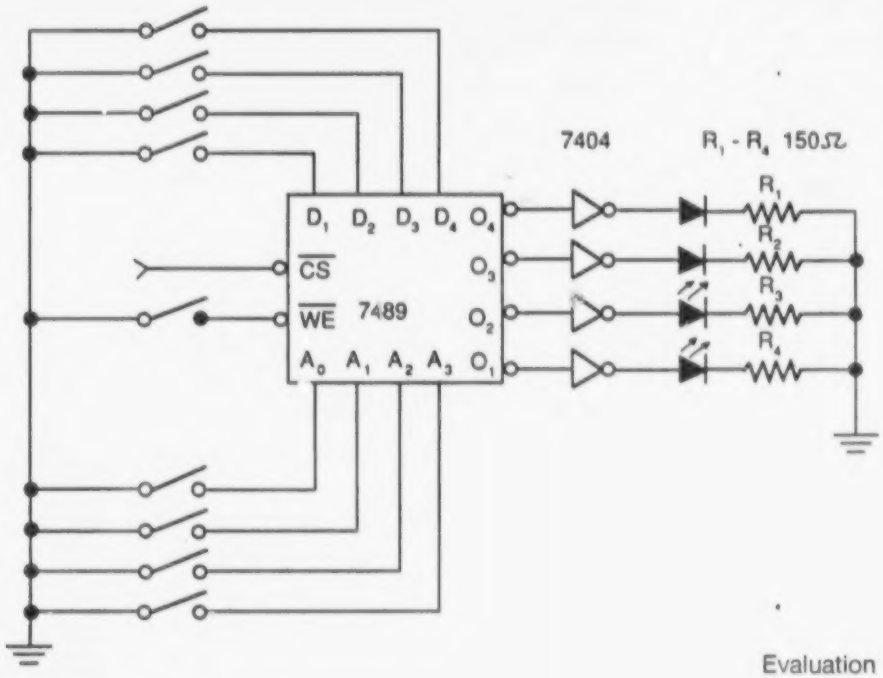
G. The selected word is not lost when data is read out. It stays in the memory register until power is removed or it is replaced by a new word.

BREADBOARD AND TEST RAM

Equipment:

7404 hex invertor I.C.
7489 RAM I.C.
LED (4)
150Ω resistor (4)
Single clock pulse
Logic switches (9)
5V DC power supply
Solderless breadboard
Logic probe
Manufacturer's data sheets for 7404 and 7408 I.C.s

NOTE: The wiring diagram for the 7489 I.C. RAM circuit is shown below. Four logic switches will be used to select the addresses of the RAM for the READ or WRITE operation. Remember that the memory enable line must be low to activate the READ/WRITE operation. A negative pulse at the enable input transfers the data to the addressed register. During the READ operation, data appears at the D1-D4 outputs in an inverted form. The 7404 I.C. invertor changes the output of D1-D4 to the normal binary output.



Procedure:

		Evaluation 3	2	1	N
1.	Place the 7404 and 7489 I.C. in the breadboard. **WARNING:** Do not connect power.	—	—	—	—
2.	Wire the circuit illustrated above.	—	—	—	—
3.	Connect DIP switches to data, address and memory inputs of the 7489 I.C.	—	—	—	—
4.	Wire four LEDs and load resistors to the output of the 7404 I.C. Check circuit for proper connections before applying power.	—	—	—	—

5 Apply power to the circuit. — — — —

6. Activate the chip select. — — — —

7. Select the read position on the write enable line by applying a low (binary 0). — — — —

8. Read the random contents of the RAM. Enter the information in binary into the table below. — — — —

Address	Register contents	Address	Register contents
0000		1000	
0001		1001	
0010		1010	
0011		1011	
0100		1100	
0101		1101	
0110		1110	
0111		1111	

9. Set the write enable line to write data into the chip. — — — —

10. Write the following data into the 7489. — — — —

Address	Data	Address	Data
0000	1111	1000	0111
0001	1110	1001	0110
0010	1101	1010	0101
0011	1100	1011	0100
0100	1011	1100	0011
0101	1010	1101	0010
0110	1001	1110	0001
0111	1000	1111	0000

11. Read the information entered in each address by selecting the proper switches. — — — —

12. Turn off power; return parts to proper locations. — — — —

Average of above evaluation* — — — —

*This average is the student's partial evaluation for competencies K6 and K11.

MODULE: DIGITAL LOGIC APPLICATION

UNIT IX: MEMORY

LESSON 2: READ ONLY MEMORY

I. Terms and definitions

A. Read-only memory (ROM)--programmed by the manufacturer during the production stage. Once programmed, the ROM cannot be reprogrammed.

B. Programmable read-only memory (PROM)--manufactured so that the purchaser can program the memory. Once the PROM has been programmed, it cannot be changed.

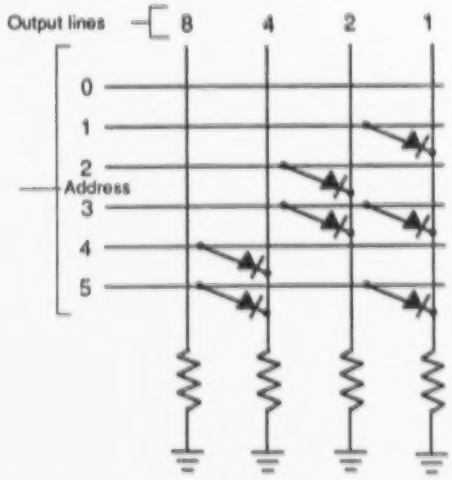
C. Erasable programmable read-only memory--can be reprogrammed repeatedly. A common type can be erased by an ultraviolet light.

II. Read-only memory (ROM)

A. ROM is used for data that can be read whenever needed, such as information on how to do repetitive computer operations. It is usually stored in a permanent memory. ROM memory is not used for data to be erased or recorded over.

B. The unit cell for the ROM is sometimes a diode.

C. The figure below represents a diode memory array. A diode in the array represents a binary 1, and a space without a diode represents a binary 0.



Truth table

8	4	2	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1

1. Mask--original layout of the diodes

2. Masking--process of making a ROM from a plan

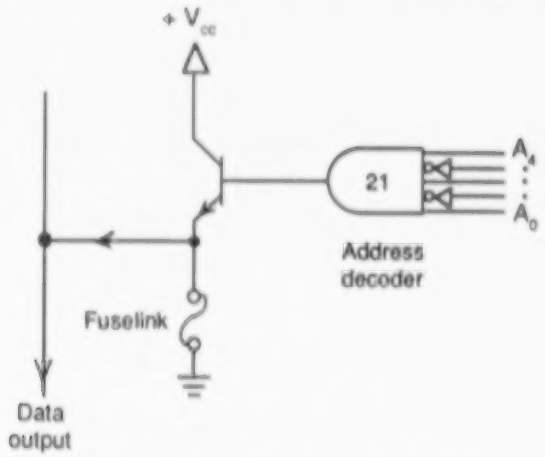
   a. Masking is accomplished by applying sufficient current through the X and Y wires to cause a silicon junction to be burned away (referred to as vaporizing a diode).

   b. When a diode is vaporized, a binary 1 is created where previously a binary 0 resided.

III. Fuse link PROM

A. Another way to store 1s and 0s in a permanent form; uses two different materials on the ROM

B. One unit cell of this type of ROM



C. Generally made of Nichrome™, an alloy of nickel and chromium made by the Driver-Harris Co.

1. Nichrome™ has more resistance and a lower melting point than the silicon in the rest of the circuit.

2. A current that is safe for the transistor is applied, which blows the fuse link.

a. When a fuse link is blown, a binary 1 is created.

b. When a fuse link is not blown, a binary 0 is created.

D. Differ from ROMs in that they can be programmed by the user. PROMs can only be programmed once. If a mistake is made, one has to start all over again with a new PROM.

IV. EPROM (the forgivable PROM)

A. If a mistake is made in the programming process, an EPROM can be erased and started over again.

B. EPROM construction processes vary from manufacturer to manufacturer.

C. To charge a memory cell, a cell is addressed and a high voltage applied to the cell for a very short period, such as 50 milliseconds. The cell retains the charge for 10 years or more.

D. Data is erased by applying a high-intensity ultraviolet light to the EPROM for approximately 20 minutes.

E. The EPROM can be protected from erasure by normal ultraviolet lighting by covering the quartz window with a piece of tape.

F. Circuit boards for programming EPROMs with a computer can be purchased reasonably for ordinary computers.

G. EPROMs can be programmed to perform many functions, giving the user a much better understanding of memory devices.

MODULE: DIGITAL LOGIC APPLICATION

UNIT IX: MEMORY

UNIT TEST

Choose the option which best answers the question or completes the statement.

___ 1. What happens when power is turned off on a ROM I.C.?

a. Data is lost
b. Data is retained
c. Address code is lost
d. ROM is refreshed
e. Data is moved

___ 2. What is the result when power is turned off on a RAM I.C.?

a. Data is lost
b. Address code is lost
c. I.C. will be damaged
d. Data is retained in memory
e. Data is moved

___ 3. The 7489 I.C. has a _____ .

a. Nonvolatile memory
b. Volatile memory
c. Diode matrix memory
d. Both a and c
e. None of the above

___ 4. The 7489 I.C. has a _____-bit memory capacity.

a. 4
b. 16
c. 64
d. 112
e. 1064

___ 5. Who normally programs ROMs?

a. The user
b. The sales store
c. The manufacturer
d. Any of the above
e. None of the above

___ 6. ROMs are not used _____ .

a. When data is continually changed
b. To erase data
c. To record over information
d. For temporary memory
e. For any of the above

___ 7. A diode memory array can usually be found in a(n) _____ .

a. RAM
b. ROM
c. PROM
d. EPROM
e. RAM or ROM

___ 8. Which is a memory device that can only be programmed one time by the user?

a. RAM
b. ROM
c. PROM
d. EPROM
e. RAM or ROM

___ 9. Which memory device can be programmed and erased by an ultraviolet light as many times as necessary?

a. RAM
b. ROM
c. PROM
d. EPROM
e. RAM or ROM

Match the appropriate term with its definition or description.

___ 10. Memory that loses its information if power is removed from it

___ 11. Process of activating an integrated circuit

___ 12. Memory that is designed to retain its information while its power is removed

___ 13. Process of locating a specific location in a memory

___ 14. Process of loading information into memory

___ 15. Binary digit

___ 16. 64-bit memory

___ 17. Process of extracting data from a certain memory location

___ 18. Memory which the purchaser can program; once it has been programmed, it cannot be changed.

___ 19. Memory which is programmed by the manufacturer during production; once programmed it cannot be reprogrammed.

___ 20. 256-bit memory

___ 21. Memory which can be reprogrammed repeatedly; a common type can be "erased" by ultraviolet light

a. 16 x 4
b. 64 x 4
c. Addressing
d. Bit
e. Enable
ab. EPROM
ac. Nonvolatile
ad. PROM
ae. RAM
bc. Read
bd. ROM
be. Write
cd. Volatile

Select the option which best answers the question or completes the statement.

___ 22. RAM circuits come in the form of integrated circuits made up of _____ .

a. Semiconductors
b. Bipolar transistors
c. Magnetic cores
d. Any of the above
e. None of the above

___ 23. Which of the following is true regarding memory capacity?

a. The number of memory locations in which data can be stored, written into or read from is commonly referred to as the number of registers.
b. K indicates the number of registers.
c. A 1K memory system has 1024 registers.
d. All of the above
e. None of the above

___ 24. A memory cell is addressed and a high voltage is applied to the cell for a very short period. This high voltage charges the cell, and the charge is retained for 10 years or more. This description is typical of a(n) _____ .

a. EPROM
b. PROM
c. ROM
d. RAM
e. All of the above

NOTE: Completion of this unit's test and job sheet to specified score is the student's final evaluation for competency K6: Describe the characteristics of ROMs and PLAs.

ANSWERS TO UNIT TEST (K6)

1. b
2. a
3. b
4. c
5. c
6. e
7. b
8. c
9. d
10. cd
11. e
12. ac
13. c
14. be
15. d
16. a
17. bc
18. ad
19. bd
20. b
21. ab
22. d
23. d
24. a

MODULE: DIGITAL LOGIC APPLICATION

UNIT X: A/D AND D/A CONVERSIONS

UNIT OBJECTIVE

Upon completion of this unit, the student should be able to describe the operation of analog-to-digital (A/D) and digital-to-analog (D/A) converters. This knowledge will be evidenced by achieving the specified score on job sheets and the unit test.

SPECIFIC OBJECTIVES

1.1 Explain D/A operation and terminology.

1.2 Explain the uses of a four-bit binary weighted DAC.

1.3 Use a manufacturer's data sheet to determine operating characteristics of a DAC. (competency K11)

1.4 Construct and test a D/A converter. (competencies K4 and K12)

2.1 Identify A/D terminology.

2.2 Explain the operation of an A/D converter.

2.3 Explain the schematic of a successive approximation ADC.

2.4 Construct and test an A/D converter. (competencies K4 and K12)

MODULE: DIGITAL LOGIC APPLICATION

UNIT X: A/D AND D/A CONVERSIONS

CONTENTS OF THIS UNIT

A. Objectives sheet

B. References

C. Notes to the instructor

D. Lesson plans

1. Lesson 1: DIGITAL-TO-ANALOG CONVERTERS (DAC)

   a. Information outline

   b. Handout

      HO 1.1: Motorola MC1408 DAC data sheet

   c. Assignment sheet

      AS 1.1: Data sheet use

   d. Job sheet

      JS 1.1: Construct and test a D/A converter

2. Lesson 2: ANALOG-TO-DIGITAL CONVERTERS (ADC)

   a. Information outline

   b. Job sheet

      JS 2.1: Construct and test an A/D converter

E. Unit test

F. Answers to unit test

REFERENCES

A. Books

1. "Digital/Microprocessor Course." Electronics Industries Asso. Consumer Electronics Group.

2. Forbes, Mark, and Barry B. Brey. Digital Electronics. Indianapolis, IN: Bobbs-Merrill Educational Publishing, 1984.

3. Kleitz, William. Digital Electronics, A Practical Approach. Englewood Cliffs, NJ: Prentice-Hall, 1987.

NOTES TO THE INSTRUCTOR

A. Suggested supplemental audiovisual

1. Analog-to-Digital and Digital-to-Analog Conversion (E-89-368). Sedalia, MO: State Fair Community College, 1987. (Available for purchase from SFCC; available for loan from Missouri Vocational Resource Center, phone 800/392-7217 or 314/882-9610)

MODULE: DIGITAL LOGIC APPLICATION

UNIT X: A/D AND D/A CONVERSIONS

LESSON 1: DIGITAL-TO-ANALOG CONVERTERS (DAC)

I. Introduction

A. Terms and definitions

1. ADC (analog-to-digital converter)

2. DAC (digital-to-analog converter)--conversion system consisting of a resistor network and summing amplifier

3. DAC accuracy--percentage difference between expected and actual output voltage; usually given by the manufacturer of the DAC. A typical accuracy is ± 0.1%.

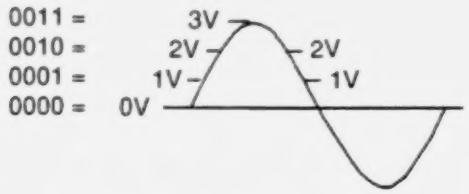
4. DAC conversion time--time required to convert a change at the inputs to the correct analog output voltage; time a computer takes to read out a coded word. (A conversion rate of 50 ns is common.)

5. DAC resolution--number of input bits the computer contains, or the reciprocal of the number of input combinations to a DAC. An eight-bit binary number has either eight bits of resolution or a resolution of 0.39% (1/256).

B. DAC converter make-up and operation

1. DACs take a binary or group of binary numbers and change them to a corresponding voltage value.

2. The figure below shows a digital chart with a sine wave and the digital BCD code necessary to produce the sine wave.



3. A binary output of 0001 can equal one volt; a binary 0010 equals two volts; a binary 0011 equals three volts, etc.

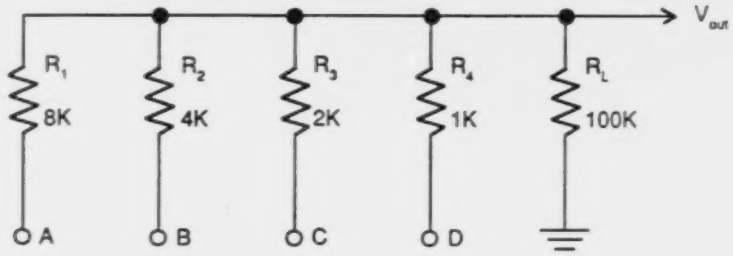
4. Digital-to-analog conversion is not a complicated process. The basic process consists of each binary number being converted to a specific analog voltage.

5. The inputs to a DAC are in the form of a weighted digital word. Depending on the type of DAC, the word used will be 4-16 bits in size.

II. Four-bit binary weighted DAC

A. There are several ways to design a DAC, but the easiest method to understand is the binary-weighted DAC. This system is made up of resistors that double in value the same way as binary numbers do from bit position to bit position.

B. The figure below shows a four-bit binary-weighted DAC.

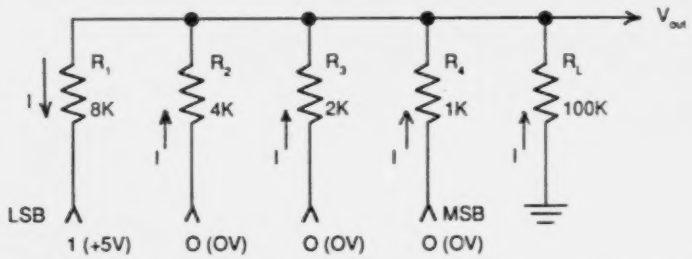


Binary Inputs

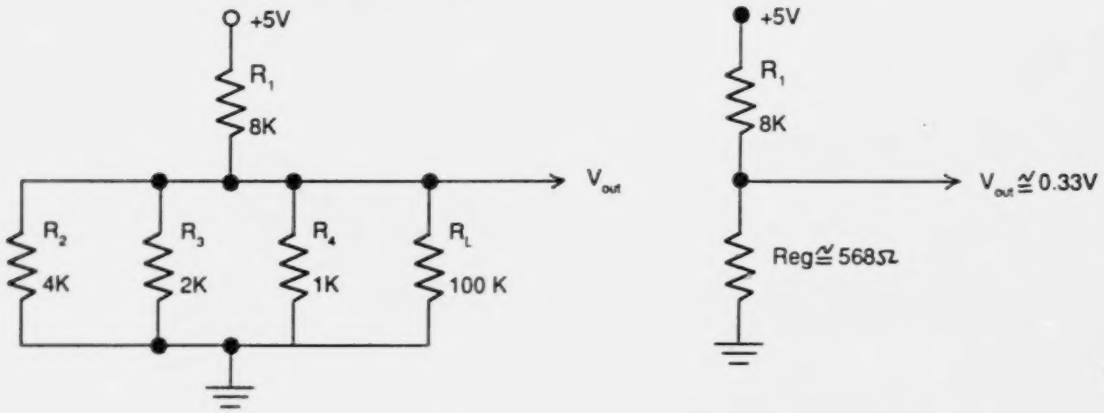
1. The four-bit binary word is applied to R_1 through R_4 with the LSB applied to R_1 and the MSB applied to R_4.

2. The load resistor (R_L) must be at least 10 times the value of the largest input resistor to provide output voltage accuracy.

C. To determine the value of each voltage step, apply the minimum binary input (0001). Using 5V for a logic 1 and 0V for a logic 0, a binary 0001 is applied to the circuit, as shown below. Notice that the LSB is applied to the largest resistor, R_1, which will result in the least current flow.

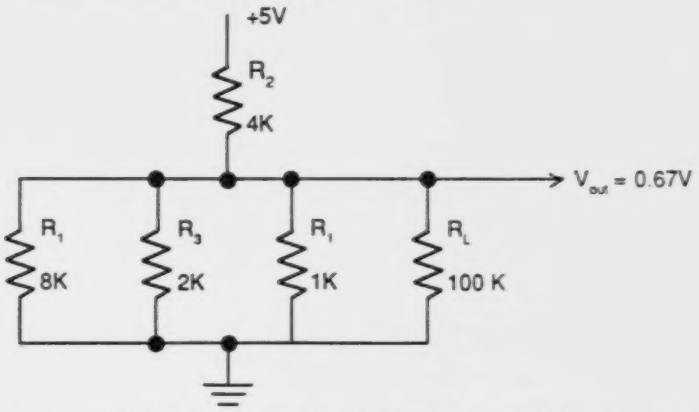


D. If the circuit is redrawn, as shown in the left illustration below, observe that R_2, R_3, R_4 and R_L are in parallel and that the equivalent resistance of this network is in series with R_8.



E. Redrawing the circuit once more (right illustration above) and using Ohm's law, the voltage drop across R_L can be determined. The V_{out} produced by the binary 0001 input is 0.33V. Since 0.33V was produced by the minimum binary input, 0.33V is the voltage step of the system.

F. For a binary 0010, the circuit should produce a V_{out} of twice the voltage step value, or approximately 0.67V. The circuit redrawn for this input is shown below.



G. Analog voltage (V_{out}) for all counts of this four-bit DAC is shown in the table below. Each binary input produces a different output voltage.

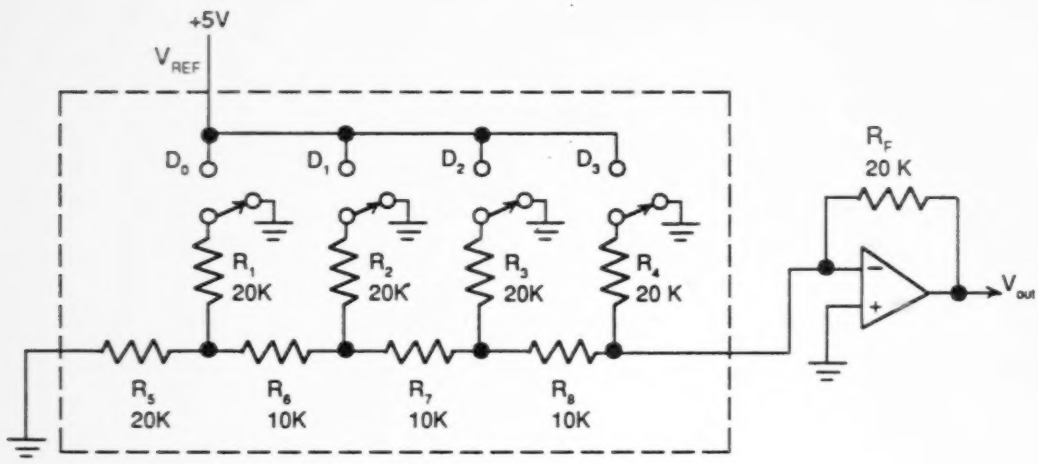
Binary count input	Analog voltage output (V_{out})	Binary count input	Analog voltage output (V_{out})
0000	0V	1000	2.67V
0001	0.33V	1001	3.00V
0010	0.67V	1010	3.33V
0011	1.00V	1011	3.67V
0100	1.33V	1100	4.00V
0101	1.67V	1101	4.33V
0110	2.00V	1110	4.67V
0111	2.33V	1111	5.00V

III. R-2R ladder DAC

A. The accuracy of the binary-weighted ladder DAC depends on the precision of the input resistors and reference voltage. A 16-bit DAC requires 16 different values of input resistors.

NOTE: Since it is impractical to build DACs from discrete parts and precision resistors cannot be manufactured within I.C.s without excessive costs, another method is required when manufacturing DACs within I.C.s, such as the R-2R ladder DAC.

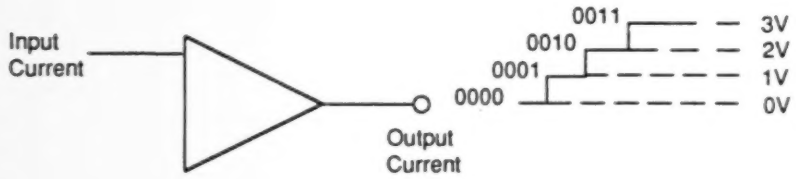
B. A more practical way of manufacturing DACs for any size of input word is to use only two different values of resistors. The circuit for this type of DAC is shown below and is called a R-2R ladder DAC circuit.



1. In the resistive ladder network shown above, five 10KΩ and three 10KΩ resistors are used.
2. Four switches represent the binary inputs.
3. Combined output of the ladder network is fed into a summing amplifier.

C. The value of each resistor is not important, but the ratio must be a 2:1 ratio between the resistors. For example, if R equals 1000Ω, 2R must equal 2000Ω.

D. The summing amplifier can convert a small current flow to an amplified voltage at its output. The figure below represents the output voltage for binary 000, 001, 010 and 011 inputs.



E. The mathematical analysis for this circuit is tedious but similar to the binary-weighted ladder circuit.

DATA SHEET FOR MOTOROLA MC1408 D/A CONVERTER

MOTOROLA

MC1408
MC1508

Specifications and Applications Information

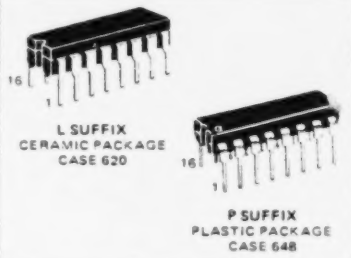
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Eight-Bit Accuracy Available in Both Temperature Ranges
  Relative Accuracy: ±0.19% Error maximum
  (MC1408L8, MC1408P8, MC1508L8)
- Seven and Six-Bit Accuracy Available with MC1408 Designated by 7 or 6 Suffix after Package Suffix
- Fast Settling Time – 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing – +0.4 V to -5.0 V
- High-Speed Multiplying Input
  Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

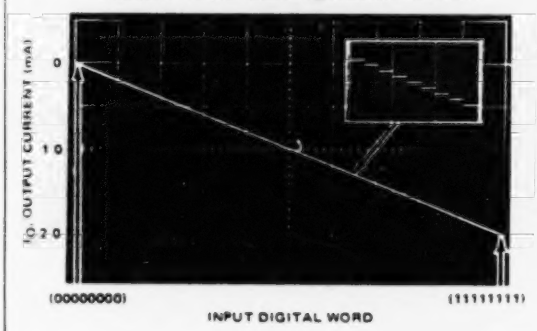
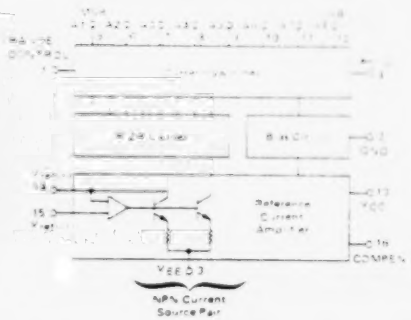


FIGURE 2 – BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

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DS 9238 R1

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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +5.5	Vdc
Applied Output Voltage	V_O	+0.5, -5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14}, V_{15}	V_{CC}, V_{EE}	Vdc
Operating Temperature Range MC1508 MC1408 Series	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, MC1508L8 T_A = -55°C to +125°C, MC1408L Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L8, MC1408L8, MC1408P8 MC1408P7, MC1408L7, See Note 1 MC1408P6, MC1408L6, See Note 1	4	E_r	 – – –	 – – –	 ±0.19 ±0.39 ±0.78	%
Settling Time to within ±1/2 LSB (includes t_{PLH}) (T_A = +25°C) See Note 2	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH}, t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	±20	–	ppm/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 – –	 0 -0.4	 0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-5.0	μA
Output Current Range V_{EE} = -5.0 V V_{EE} = -15 V, T_A = 25°C	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	1.9	1.99	2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4.0	μA
Output Voltage Compliance ($E_r \leq 0.19\%$ at T_A = -25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0.55, +0.4 -5.0, +0.4	Vdc
Reference Current Slew Rate	6	SR I_{ref}	–	4.0	–	mA/μs
Output Current Power Supply Sensitivity		PSRR(–)	–	0.5	2.7	μA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Dissipation All bits low V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_D	 – – – –	 105 190 90 160	 170 305 – –	mW

Note 1. All current switches are tested to guarantee at least 50% of rated output current.
Note 2. All bits switched.

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DATA SHEET USE

Read the reference material and data sheets for the MC1408 D/A converter (HO 1.1). Then answer the following questions.

1. How many bits are used with the MC1408?

2. What is the resolution?

3. What are the maximum V_{CC} and V_{EE} values?

4. What are the typical operating values for V_{CC} and V_{EE}?

5. Are the digital inputs TTL compatible?

6. What should be done with pin 1 for a V_{EE} value below -10V?

7. What is the typical full-scale output current when a voltage reference of 2V and R14 equals 1KΩ?

NOTE: · Completion of this assignment sheet to specified score is the student's final evaluation for competency K11: Use data sheets.

ANSWERS TO ASSIGNMENT SHEET

1. 8
2. 1/256
3. V_{CC} = +5.5V, V_{EE} = -16.5V
4. V_{CC} = +5V, V_{EE} = -5.0V to -15V
5. Yes
6. Open
7. 1.99mA

CONSTRUCT AND TEST A D/A CONVERTER

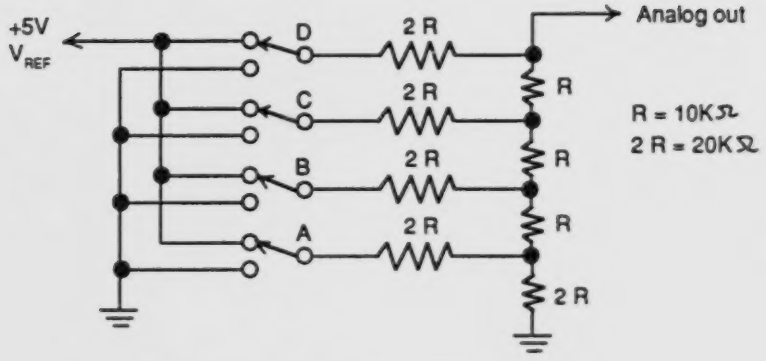
Equipment:

10KΩ, 1/4 watt resistors (3)
20KΩ, 1/4 watt resistors (5)
7490 decade counter I.C.
7448 BCD to seven-segment decoder I.C.
Common cathode seven-segment display
74LS244 octal buffer I.C.
4.7KΩ resistor, 1/4 watt
DC power supply
Voltmeter
TTL square wave generator
Oscilloscope
Logic pulser

Procedure:

Evaluation 3 2 1 N

1. Connect the R-2R ladder DAC below. — — — —



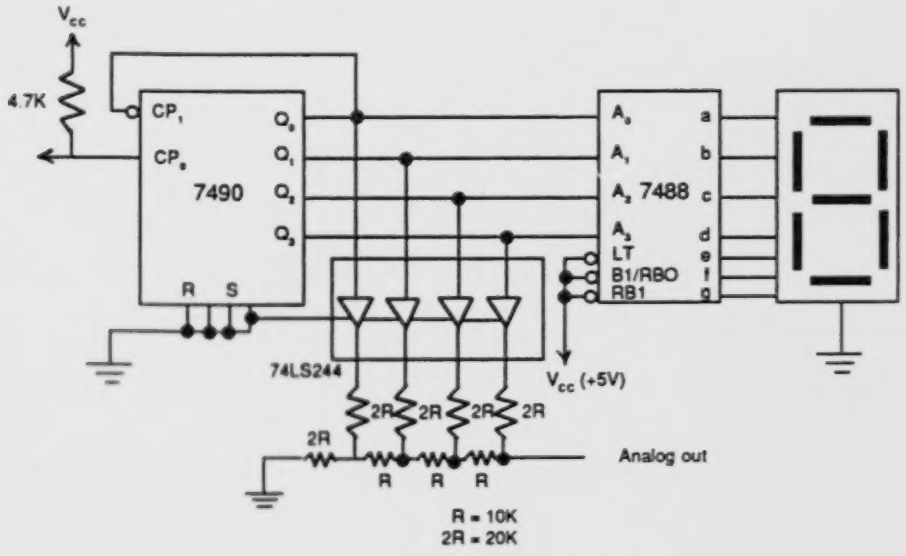
Circuit #1

2. Apply power to the circuit. Verify correct voltage. — — — —

3. Connect a voltmeter to the analog output. Record the analog voltage as switches are adjusted from 0 through 9; record the voltages in the chart that follows. — — — —

	D	C	B	A	Circuit #1	Circuit #2
0.	0	0	0	0		
1.	0	0	0	1		
2.	0	0	1	0		
3.	0	0	1	1		
4.	0	1	0	0		
5.	0	1	0	1		
6.	0	1	1	0		
7.	0	1	1	1		
8.	1	0	0	0		
9.	1	0	0	1		

4. Remove power and connect the circuit below. — — — —



Circuit #2

5. Apply power. Connect a voltmeter to the analog output. — — — —

6. Using a logic pulser, step the 7490 I.C. through its count (0-9) and record the analog voltage output for each count in the chart above (Circuit #2). — — — —

7. Apply a 100 Hz TTL square wave to the clock input of the 7490 I.C. — — — —

8. Connect an oscilloscope to analog output. Sketch the resulting waveform below. — — — —

9.	Dismantle the circuit. Return equipment and materials to the proper storage area.	—	—	—	—
Average of above evaluations*		—	—	—	—

*This average is the student's partial evaluation for competencies K4 and K12.

MODULE: DIGITAL LOGIC APPLICATION

UNIT X: A/D AND D/A CONVERSIONS

LESSON 2: ANALOG-TO-DIGITAL CONVERTERS (ADC)

I. Terms and definitions

A. Absolute accuracy error--difference between the theoretical analog input required to produce a given output code and the actual analog input required to produce the same code

B. Conversion speed--speed at which a converter can make repetitive conversions

C. Conversion time--time required for a complete conversion cycle of an ADC. Conversion time is the function of the number of bits and the frequency.

D. Differential non-linearity--deviation in the range of inputs from one LSB that causes the output to change from one given code to the next, usually in the form of a missing code.

E. Missing code--code combination that does not appear in the ADC's output range

F. Offset error--difference between the input level that causes the first code transition and what that level should be

G. Relative accuracy--measure of the difference of the theoretical output value with a given input after any offset and gain errors have been nulled out

H. Resolution--number of bits at the input or output of an ADC or DAC. It is the number of discrete steps or states at the output.

I. Transfer characteristic--relationship of the output to the input (D_{out} vs. A_{in})

J. Quantizing--quantity that is composed of discrete values

K. Quantizing error--In an ADC there is an infinite number of possible input levels but only 2^n output codes (n = number of bits). There will be, therefore, an error in the output code that could be as great as 1/2 LSB because of the quantizing effect.

II. ADC process

A. Analog-to-digital conversion is a more complex process than digital-to-analog conversion. Analog-to-digital conversion begins with a continuous voltage. The ADC must quantize this continuous voltage into specific digital values.

B. There are four common methods used in converting analog voltages to digital values. The four types of ADCs are the counter/ramp, dual slope, successive approximation and flashADC.

1. **Counter/ramp**--uses an up/down counter to enable the ADC to continually track the input voltage. This ADC is used in medium-speed circuits.

2. **Dual slope**--slowest analog-to-digital conversion. It is widely used, however, because of its simplicity, accuracy and minimum cost. It has excellent noise immunity and is used in most digital meters.

3. **Successive approximation**--This ADC and the dual slope ADC circuits are used in approximately 90% of all ADCs. The high performance, two-step successive

approximation ADC changes two bits at a time, which doubles the conversion speed. This ADC is used in medium- to high-speed requirements.

4. **FlashADC**--also known as simultaneous/parallel ADC. This ADC's complexity limits its use to primarily video circuits in excess of 20 MHz. (For example, an eight-bit flashADC requires 255 comparators, 256 precision resistors and 255 encoders.)

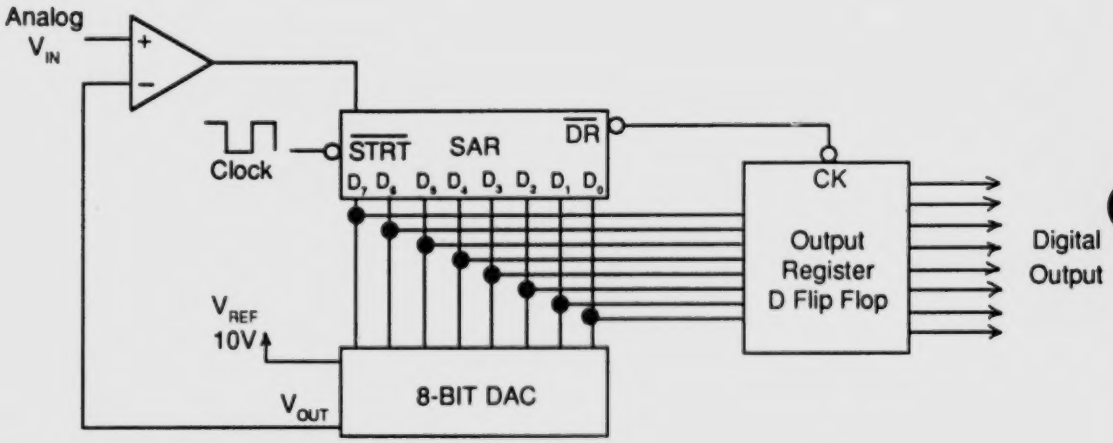
III. Successive approximation ADC operation

A. Successive approximation ADCs employ a D/A converter connected to a successive approximation register (SAR) that stores a binary equivalent of half the full scale output of the converter.

B. Both the converter output and the incoming analog signal are fed into the comparator. If the D/A converter's output is less than the input signal, the most significant bit (MSB) in the data register remains high. The next most-significant bit goes high when the next clock pulse arrives.

C. The updated output from the D/A converter is then compared with the input signal. If it is greater than the input, the second most significant bit goes high.

D. The figure that follows shows a simplified SAR analog-to-digital converter.



E. Conversion begins when the $\overline{\text{STRT}}$ line goes low.

1. The SAR first tries a high on the MSB (D7) line to the DAC. D7 will cause the DAC to output half its full-scale output.

2. If the DAC output is higher than the unknown analog input voltage, the SAR returns the MSB low.

3. If the DAC output was still lower than the unknown analog input voltage, the SAR leaves the MSB high.

F. The next lower bit (D6) is tried. If a high on D6 causes the DAC output to be higher than the input analog voltage, it is returned low. If it is not, it is left high.

G. This action continues until all bits have been tried. At the end (eight bits tested), the SAR will contain an eight-bit binary number that represents the analog input. The $\overline{\text{DR}}$ output goes low when the conversion is complete and the clock pulse loads the data into the D flip-flops for output on the Q_0 to Q_7 lines.

CONSTRUCT AND TEST AN A/D CONVERTER

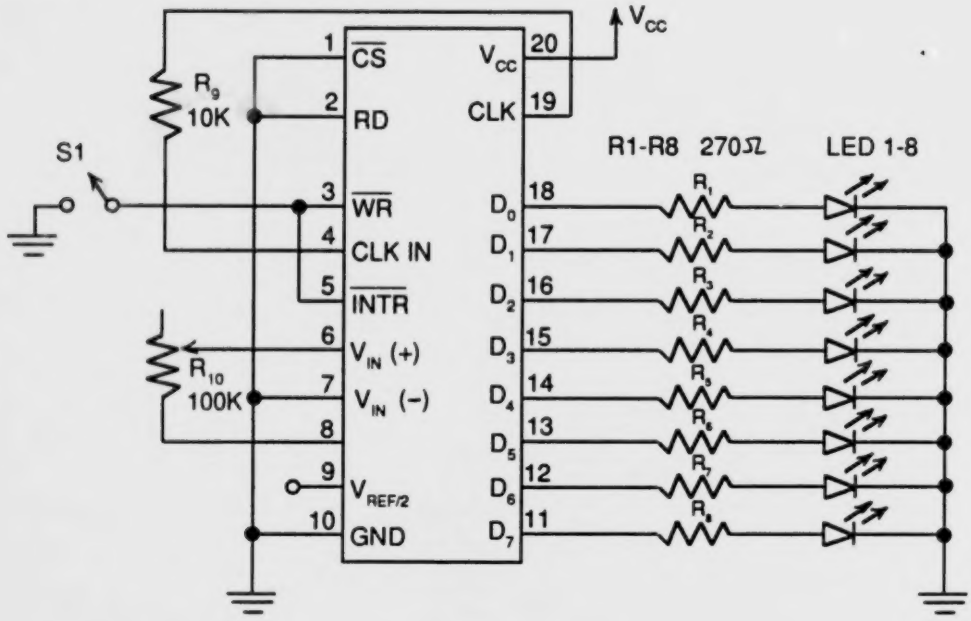
Equipment:

Voltmeter
Solderless breadboard
Power supply, DC
ADC 0804 A/D converter I.C.
LEDs (8)
270Ω resistors, 1/4 W (8)
10KΩ resistor, 1/4 W
100KΩ trim potentiometer
150 pF capacitor
SPST switch

NOTE: The ADC0804 is a TTL-compatible CMOS eight-bit successive approximation A/D converter that is used to convert analog voltage to an eight-bit binary number. In this exercise the student will use an analog voltage taken from R10 and convert it to a digital value.

Procedure:

	Evaluation 3	2	1	N
1. Connect the circuit shown below.	—	—	—	—



2. Apply power to the circuit after checking correctness of wiring.	—	—	—	—
3. Verify correctly applied voltages. Monitor the analog voltage at pin 6 with a voltmeter.	—	—	—	—
4. Adjust R_{10} so that the analog input voltage is 2.5V.	—	—	—	—
5. Connect a digital probe on pin 3 or 5. If there is no activity, momentarily close S1 (ensures the start-up of the conversion process).	—	—	—	—
6. With an analog input of 2.5V, what is the digital output? _____	—	—	—	—

7. Record the analog voltage and digital output for several settings of R_{10}. — — — —

Analog voltage (pin 2) Digital output (binary)

8. Remove power. An analog voltage can be mathematically calculated from a digital output by using the following procedure. — — — —

a. Change the digital number to a decimal number.

b. Divide the decimal number by 256.

c. Multiply the result by the reference voltage (5V).

d. Convert the digital output in step 7 to the analog input by using this process.

$$V = \frac{\text{ADC output} \times 5}{256}$$

Average of above evaluations* — — — —

*This average is the student's final evaluation for competencies K4 and K12.

MODULE: DIGITAL LOGIC APPLICATION

UNIT X: A/D AND D/A CONVERSIONS

UNIT TEST

Select the option which best answers the question or completes the statement.

____ 1. Which of the following is an interface device that converts analog to digital?

a. DAC
b. ADC
c. TTL
d. MOS
e. CAD

____ 2. Which is an interface device that converts digital to analog?

a. DAC
b. ADC
c. TTL
d. MOS
e. IDC

____ 3. What does a DAC consist of?

a. Encoder and decoder
b. Scaling amplifier and decoder
c. Resistor network and summing amplifier
d. Op-amp and two resistors
e. b and c

____ 4. An eight-bit binary number has a resolution of _____ .

a. 1/8
b. 1/16
c. 1/64
d. 1/112
e. 1/256

____ 5. What is the most commonly used ADC?

a. Flash
b. Successive approximation
c. Dual slope
d. Counter/ramp
e. None of the above

____ 6. A DAC takes binary numbers or combinations of binary numbers and changes them to _____ .

a. Hex numbers
b. Hex or octal numbers
c. Corresponding voltage values
d. A seven-segment display device
e. Corresponding analog values

___ 7. What is the summing amplifier used for in DAC circuits?

a. Filter the digital signals
b. Amplify the binary numbers
c. Add two or more binary numbers
d. Convert small binary number into analog voltages
e. Convert digital signals to binary

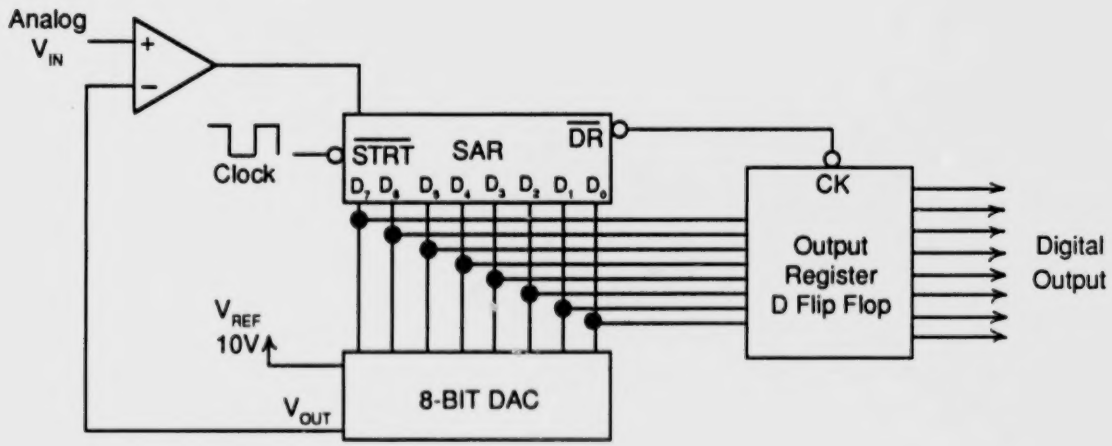
___ 8. Which of the following is relatively easy to understand and is made up of resisters that double in value like binary numbers do?

a. FlashADC
b. Successive approximation ADC
c. R-2R ladder DAC
d. Four-bit binary weighted DAC
e. None of the above

___ 9. Beginning with a continuous voltage, what quantizes this voltage into specific digital values?

a. DAC
b. ADC
c. TTL
d. MOS
e. CAD

___ 10. What kind of converter does the following schematic describe?



a. FlashADC
b. Simplified successive approximation register
c. R-2R ladder DAC
d. Four-bit binary weighted DAC
e. None of the above

Match the following terms and definitions.

___ 11. Number of bits at the input or output of an ADC or DAC. It is the number of discrete steps or states at the output.

___ 12. Difference between the theoretical analog input required to produce a given output code and the actual analog input required to produce the same code

___ 13. Difference between the input level that causes the first code transition and what that level should be

___ 14. Measure of the difference of the theoretical output value with a given input after any offset and gain errors have been nulled out

___ 15. Quantity that is composed of discrete values

___ 16. Relationship of the output to the input (D_{out} vs. A_{in})

___ 17. Deviation in the range of inputs from one LSB that causes the output to change from one given code to the next, usually in the form of a missing code.

a. Absolute accuracy error

b. Conversion speed

c. Differential non-linearity

d. Digital-to-analog converter

e. Offset error

ab. Quantizing

ac. Relative accuracy

ad. Resolution

ae. Transfer characteristic

ANSWERS TO UNIT TEST (K12)

1. b
2. a
3. c
4. e
5. b
6. c
7. d
8. d
9. b
10. b
11. ad
12. a
13. e
14. ac
15. ab
16. ae
17. c